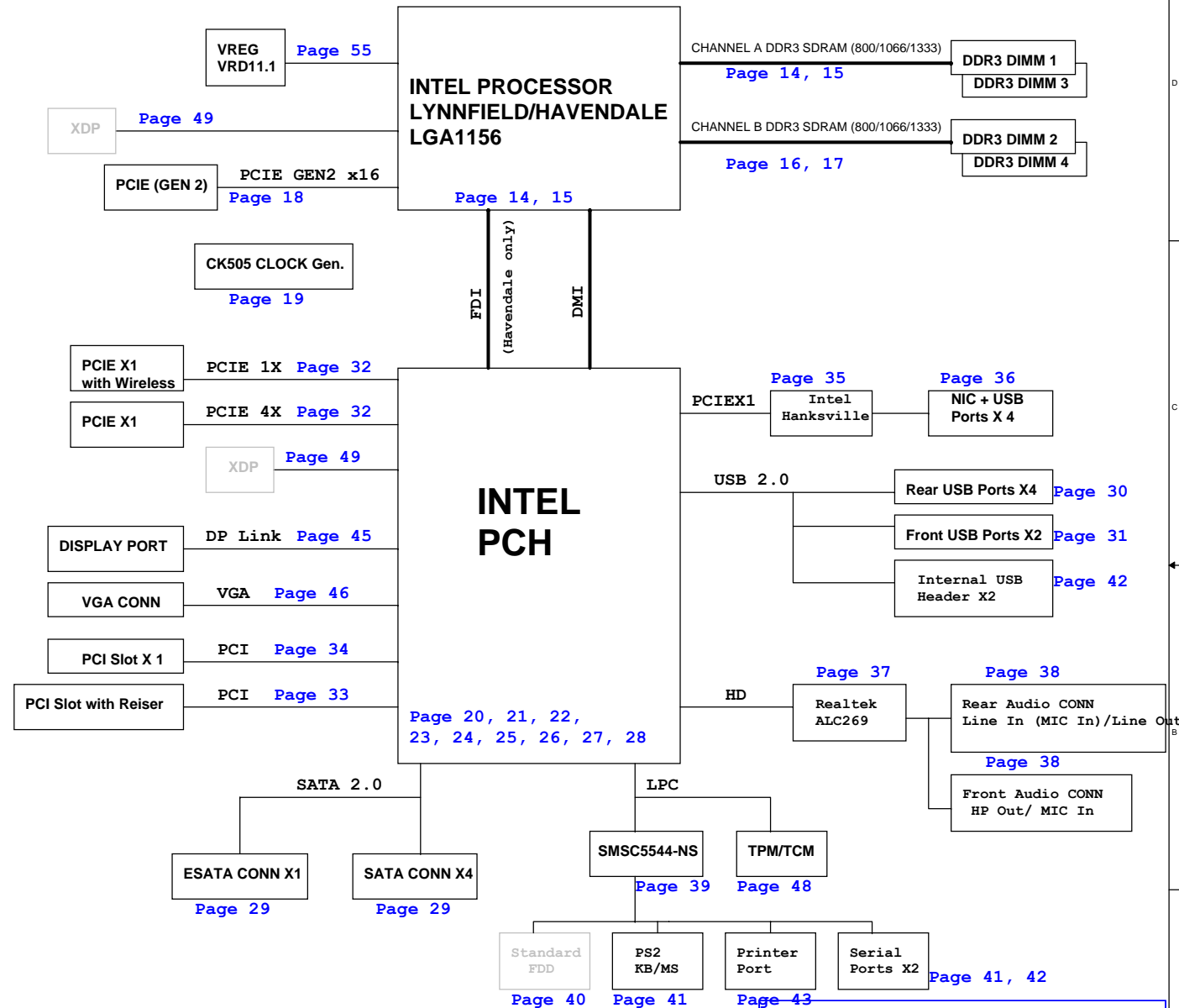


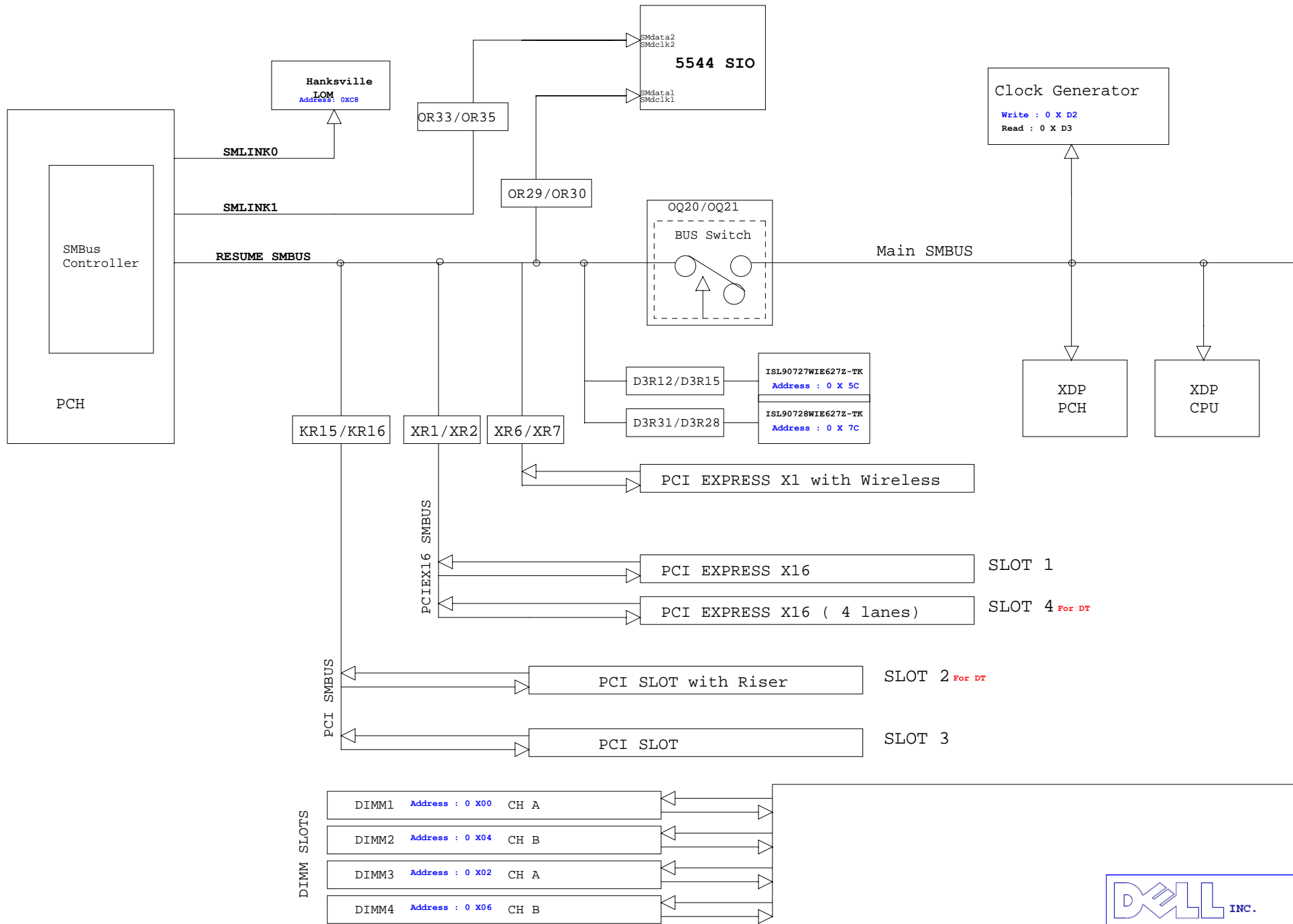
1. Index / Block diagram
2. SMBus MAP
3. Clock Distribution
4. Power Delivery Map
5. Power On Sequence
6. Reset / Power Good Map
7. GPIO/IRQ/IDSEL TABLE
- 8-13. CPU
- 14-15. DDR3:CHA
- 16-17 DDR3:CHB
- 18 .PCIE X16 SLOT
19. CLOCK GEN
- 20-28. PCH
29. SATA CONNECTOR
30. REAR USB CONNECTOR
31. FRONT USB HEADER
32. PCIE X1 SLOT
- 33-34. PCI SLOT
35. LAN:INTEL HANKSVILLE
36. LAN:CONNECTOR WITH USB/POWER
- 37-38. AUDIO:ALC269
- 39-40. SIO:SMSC5544NS
41. COM Port/PS2
42. Front I/O & COM2 HDR
43. PRT Port
44. FAN
45. DISPLAY PORT
46. VGA
47. SPI
48. TPM/TCM
49. XDP
50. BUZ / CLR PSWD/LPC DEBUG
51. ATX Power CONN /Floppy
52. POWER SEQUENCE
- 53-54. POWER:LINEAR POWER REGULATOR
- 55-58. POWER:SWITCH POWER REGULATOR
59. EMI
60. Change List
61. GPIO PIN



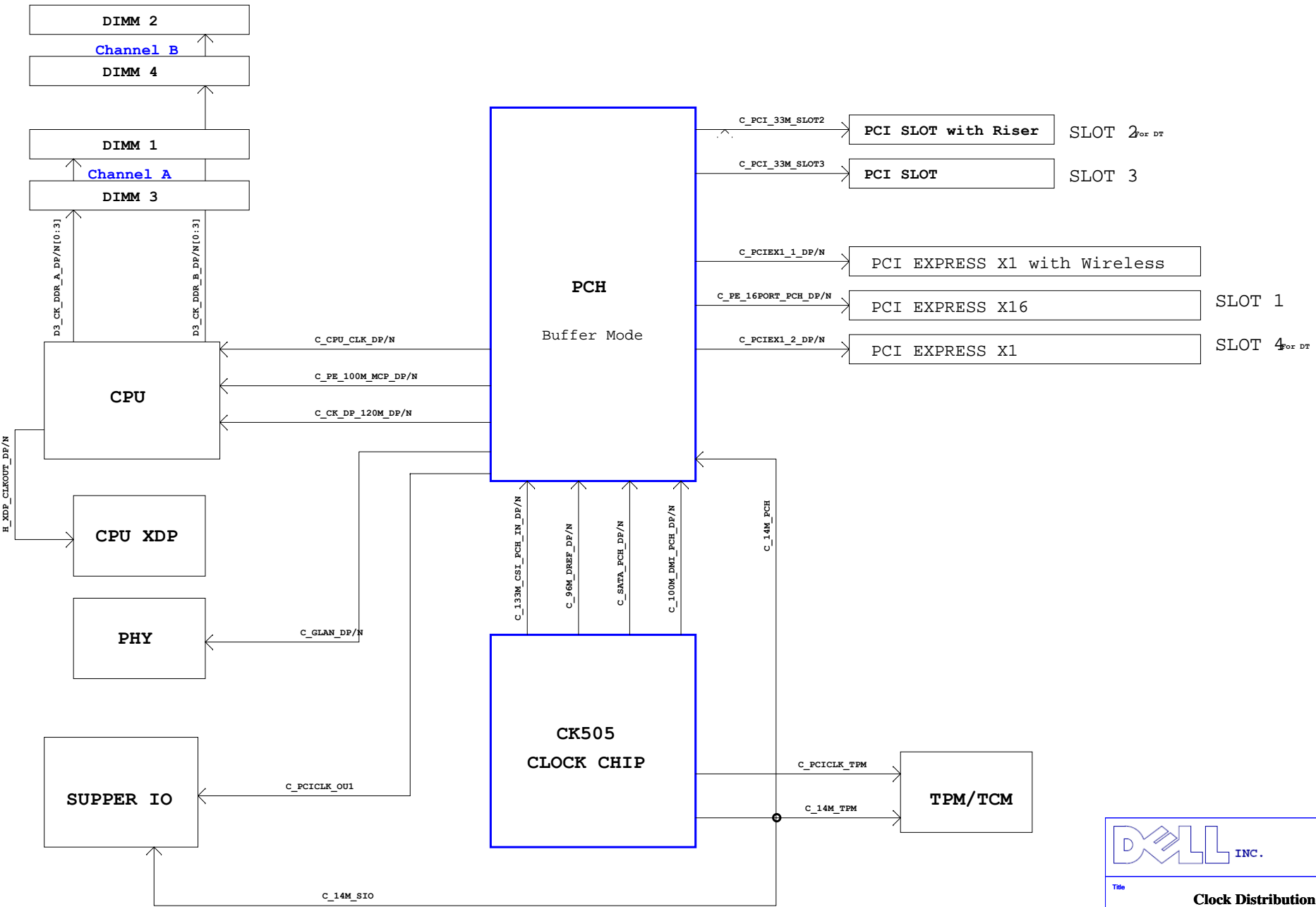
DESIGN	CHECK	APPROVE
Hiko Pan Ronie Ko	Ivan	Ping-kun

DELL INC.	
Title	
Cover Sheet	
DWG NO	Rev
Wembley_MT	A01
Date: Wednesday, April 14, 2010	Sheet 1 of 61

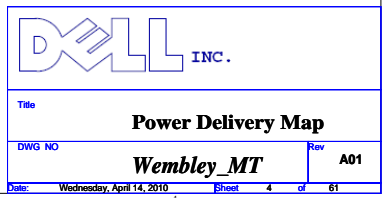
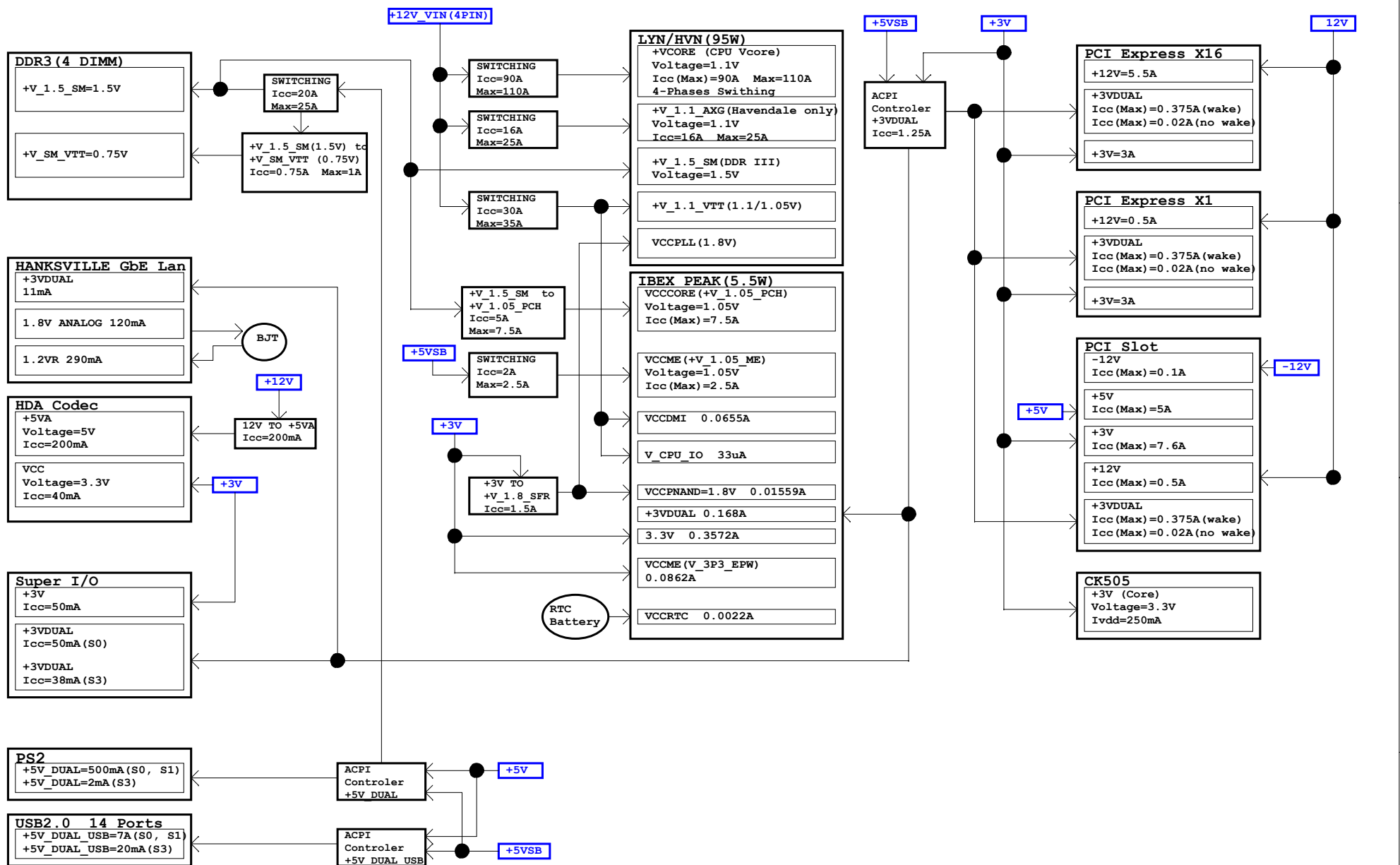
SMBUS DIAGRAM



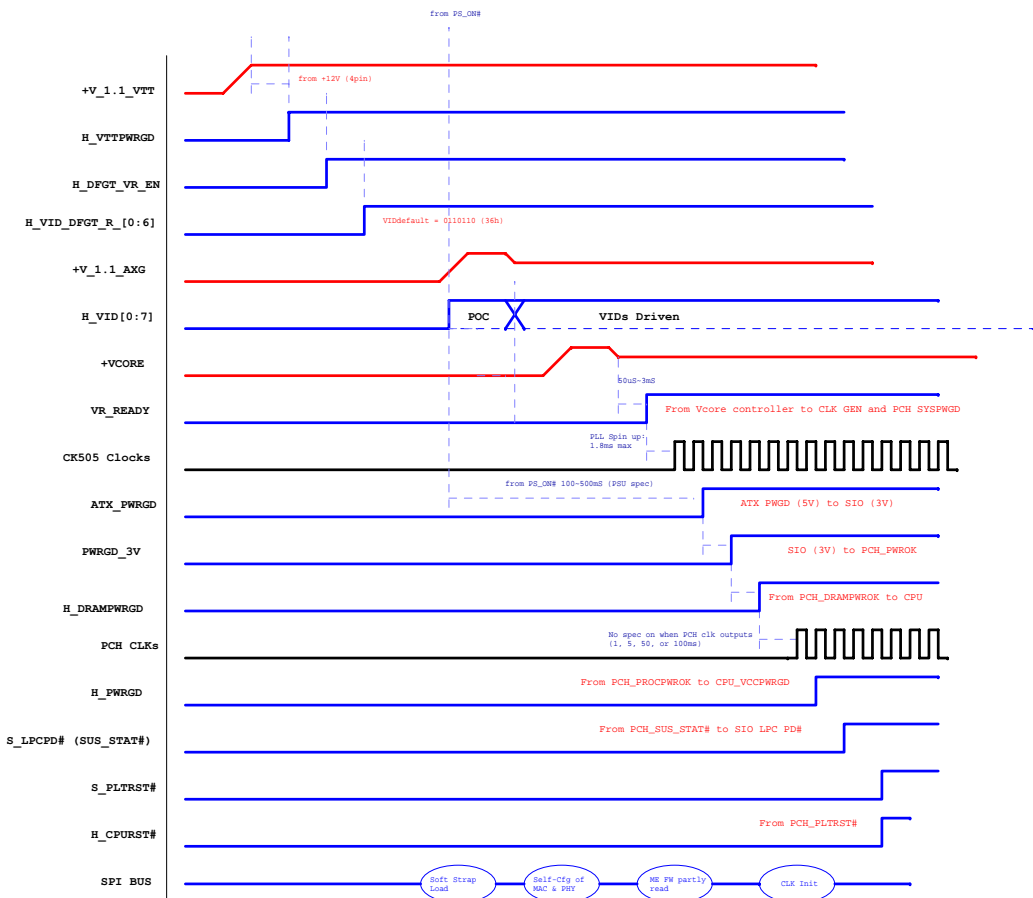
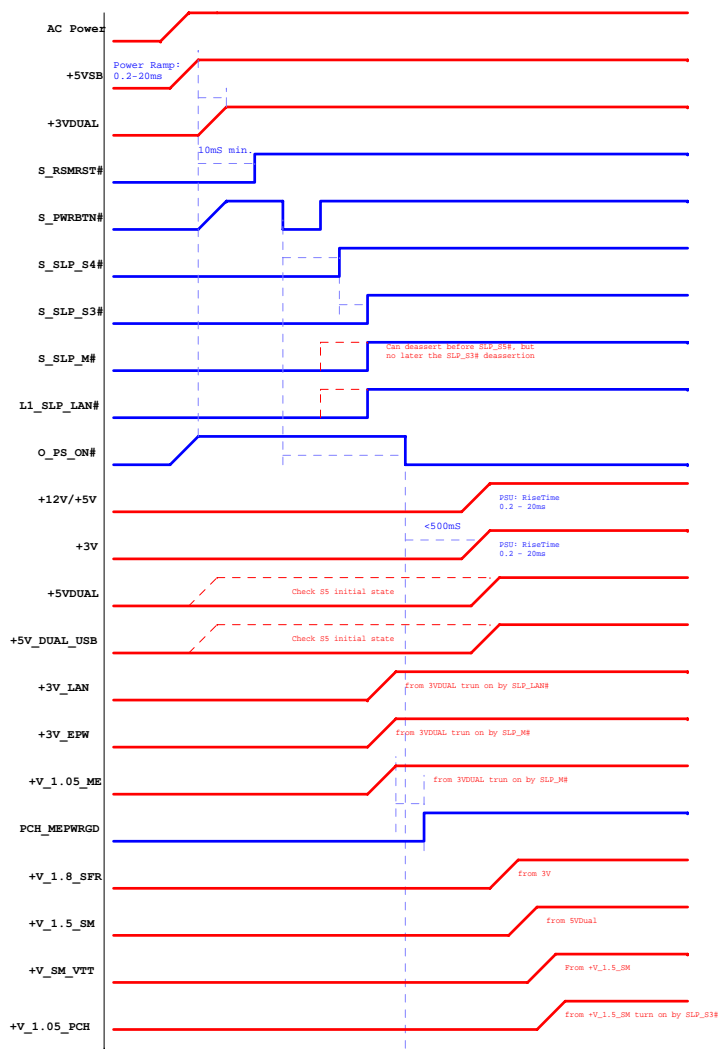
CLOCK DISTRIBUTION



POWER DELIVERY MAP



POWER ON SEQUENCE



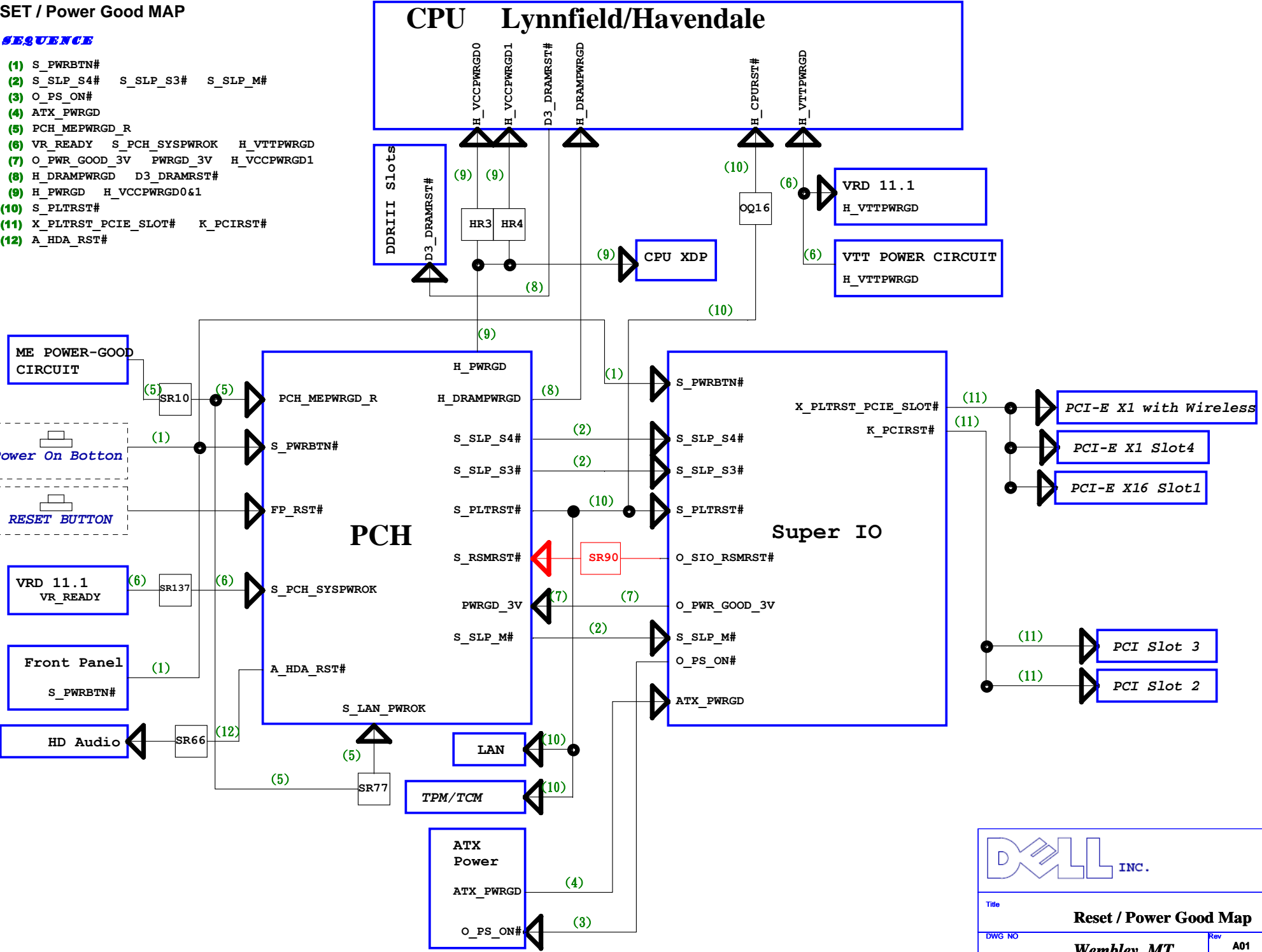
Black Line --> Clocks
Blue Line --> Logical State
Red Line --> Power Rails

RESET / Power Good MAP

CPU Lynnfield/Havendale

SEQUENCE

- (1) S_PWRBTN#
- (2) S_SLP_S4# S_SLP_S3# S_SLP_M#
- (3) O_PS_ON#
- (4) ATX_PWRGD
- (5) PCH_MEPWRGD_R
- (6) VR_READY S_PCH_SYSPWROK H_VTTPWRGD
- (7) O_PWR_GOOD_3V PWRGD_3V H_VCCPWRGD1
- (8) H_DRAMPWRGD D3_DRAMRST#
- (9) H_PWRGD H_VCCPWRGD0&1
- (10) S_PLTRST#
- (11) X_PLTRST_PCIE_SLOT# K_PCIRST#
- (12) A_HDA_RST#



IRQ Routing Table

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot2	A	B	C	D	16	0	0
Slot3	C	D	A	B	18	2	2
Riser	B	C	D	A	17	1	1

STRAPPING Table

CPU side

H_CPU_CFG	H	L	Description
0	See PEG Config Table		PEG SEL0
1			PEG SEL1
2			PEG SEL2
3	Normal	Reversed	LANE Reversal Default
4	Disable	Enable	DP Presence Default
5	RSVD		
6	RSVD		
7	RSVD		
15	RSVD		

PEG Config Table

PEG SEL2	PEG SEL1	PEG SEL0	PEG Config
1	1	1	1 X 16 Default
1	1	0	2 X 8

Clock Gen.

FREQ	C_CK_BSEL0	C_CK_BSEL0	C_CK_BSEL0
100	1	0	1
133	1	0	0 Default

PIN NAME	NET		Strapping description
PCI2/TME (PIN4)	CK_PIN4	1	Overclocking DISABLED DEFAULT
		0	Overclocking ENABLED
PCI3/CFGFP (PIN5)	CK_PIN5	1	CGF TABLE ENABLED
		0	CGF TABLE DISABLED DEFAULT
PCI4/SRC5_EN (PIN6)	CK_PIN6	1	SRC5 DEFAULT
		0	CPU_STOP# and PCI_STOP#
PCI_F5/ITP_EN (PIN7)	CK_PIN7	1	CPU_ITP
		0	SRC8 DEFAULT

SIO SMSC5544 Functional Straps

PIN NAME	NET		Strapping description
GP070 / PWM4 (PIN127)	O_SPEAKER	1	Diag_En Disable
		0	Diag_En Enable DEFAULT
DTR1# [TEST_EN] /GP051 (PIN104)	O_DTR1#	1	PE BOOT Loader Strap (DTR1#)= Load from SPI
		0	PE BOOT Loader Strap (DTR1#)= No Load from SPI DEFAULT

On-Die PLL Voltage Regulator Voltage Select

HAD_SYNC	Description
High	1.5V
Low	1.8V

DEFAULT

On-Die PLL Voltage Regulator

GPIO27	Description
High	Regulator is enabled.
Low	Regulator is disabled.

DEFAULT

Topblock swap mode

GNT3# (Inernal pull up)	Description
High	Topblock swap mode: Disable
Low	Topblock swap mode: Enable

DEFAULT

No reboot mode

SPKR (Inernal pull down)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable

DEFAULT

Integrated 1.1V VRM

INTVRMEN	Description
High	Integrated 1.1V VRM: Enable
Low	Integrated 1.1V VRM: Disable

DEFAULT

Intel- Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable

S_NVR_ALE	Description
High	Anti-Theft Technology: Enable
Low	Anti-Theft Technology: Disable

DEFAULT

Intel Management Engine features (S_MFG_MODE#)

GPIO33	Description
High	Intel Management Engine: Enable
Low	Intel Management Engine: Disable

DEFAULT

TPM Functionality

SPI_MOSI (Inernal pull down)	Description
High	TPM Functionality: Enable
Low	TPM Functionality: Disable

DEFAULT

DMI termination voltage

NV_CLE (Inernal pull down)	Description
High	DMI termination voltage : Enable
Low	DMI termination voltage : Disable

DEFAULT

Boot BIOS Destination Selection

GNT1# (Inernal pull up)	GNT0# (Inernal pull up)	Description
Low	High	Reserved
High	Low	Flash cycle routed to PCI
High	High	Flash cycle routed to SPI
Low	Low	Flash cycle routed to LPC

DEFAULT



Title

GPIO/IRQ/IDSEL Table

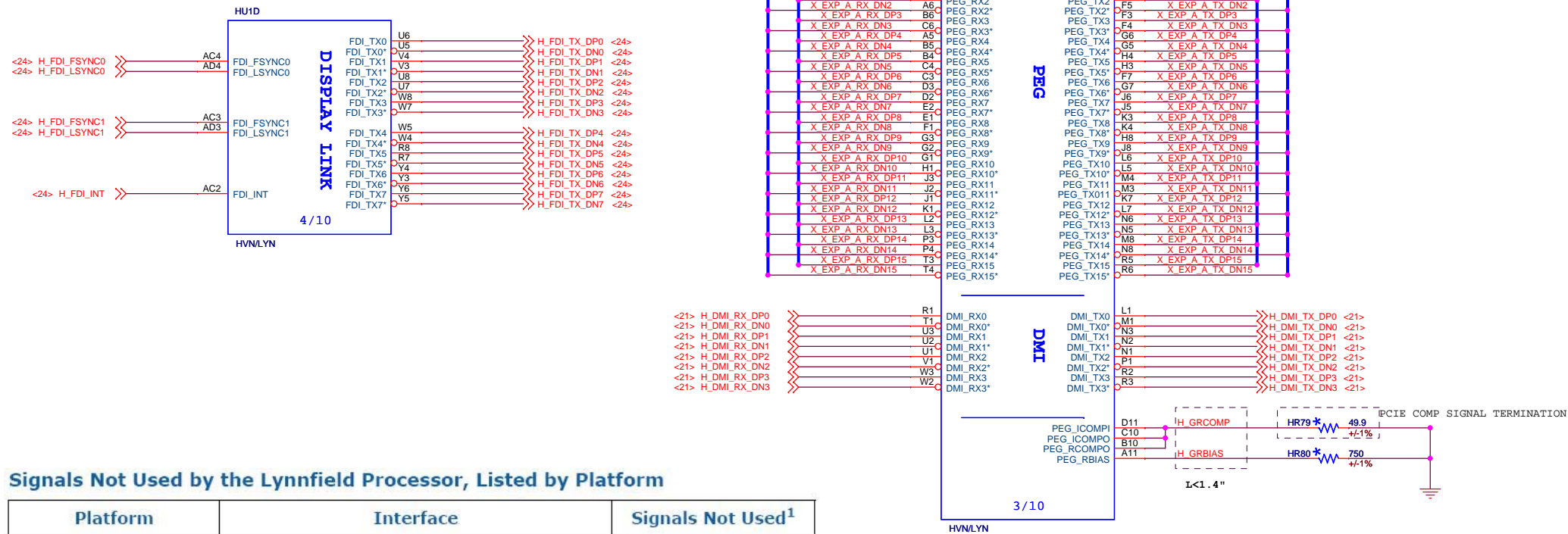
DWG NO

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Rev

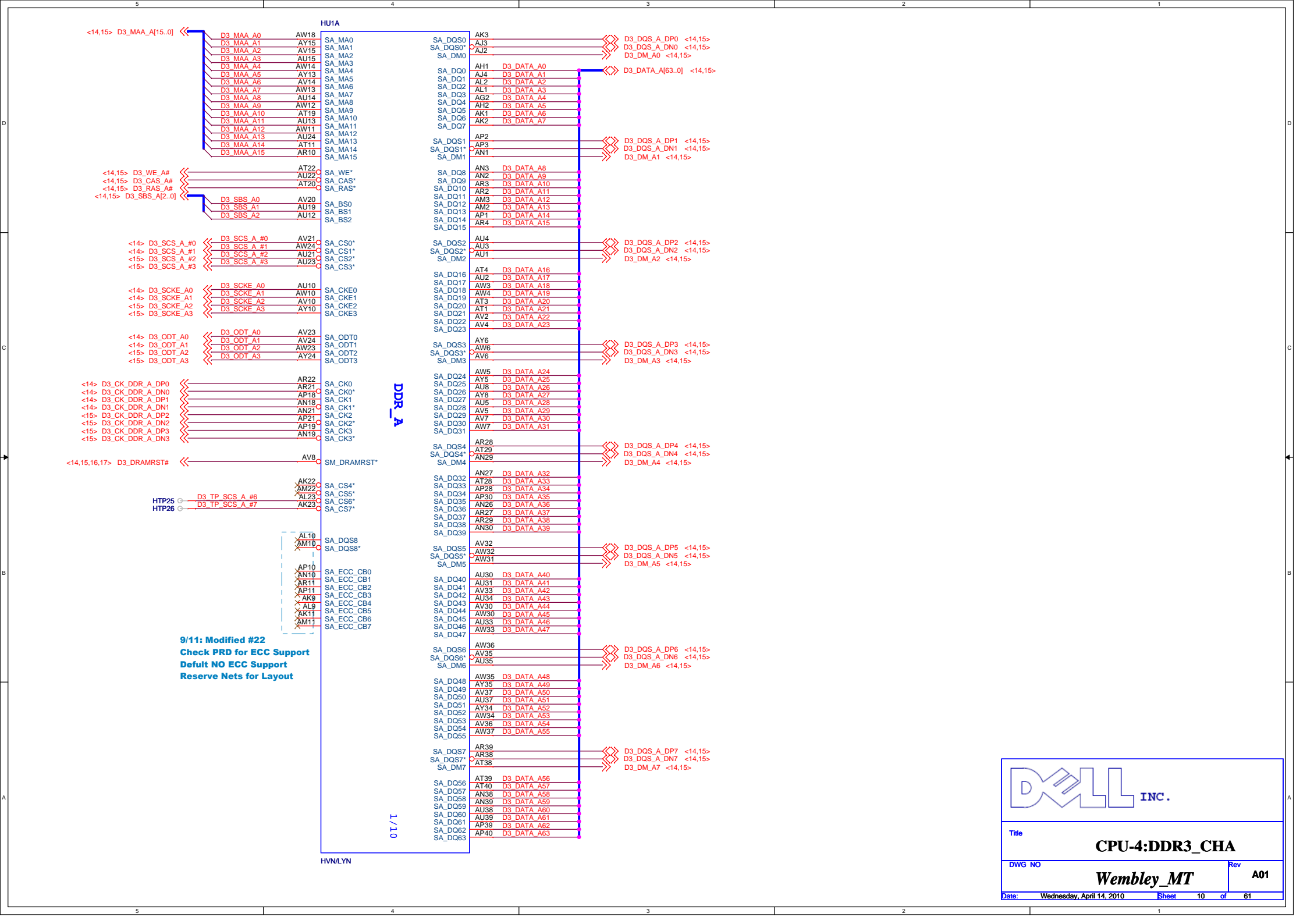
A01

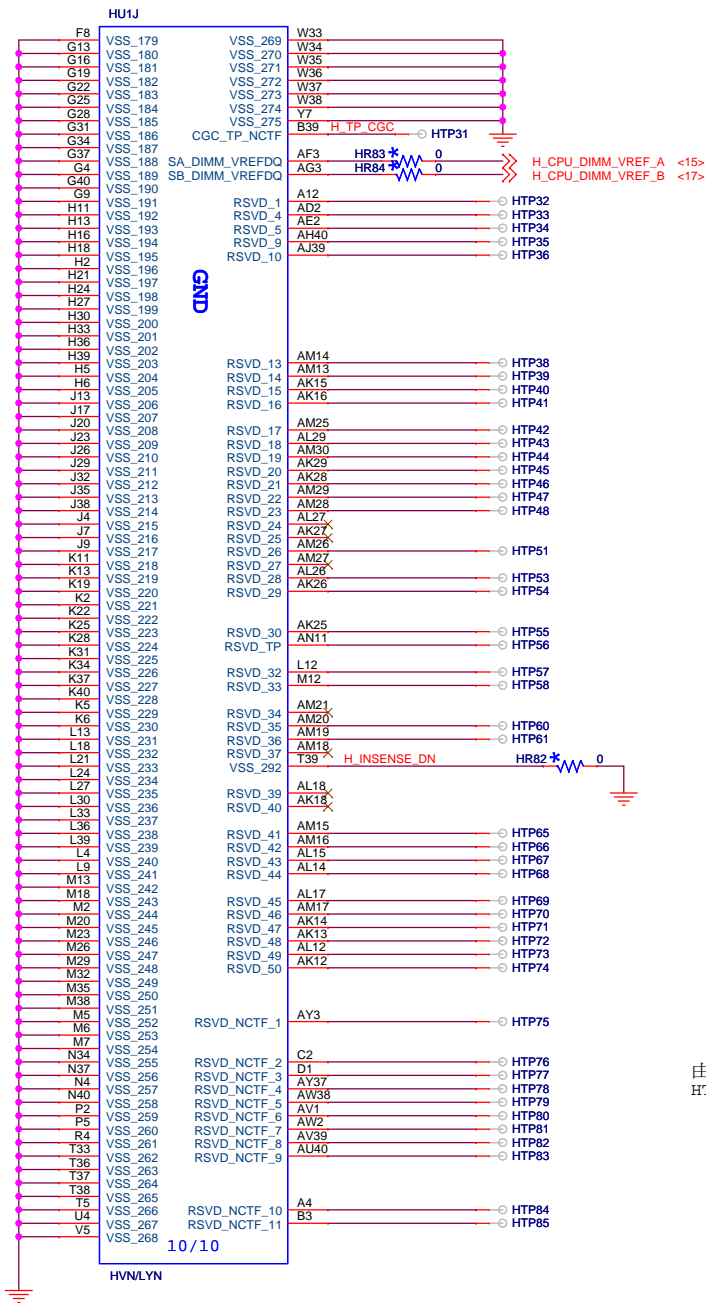
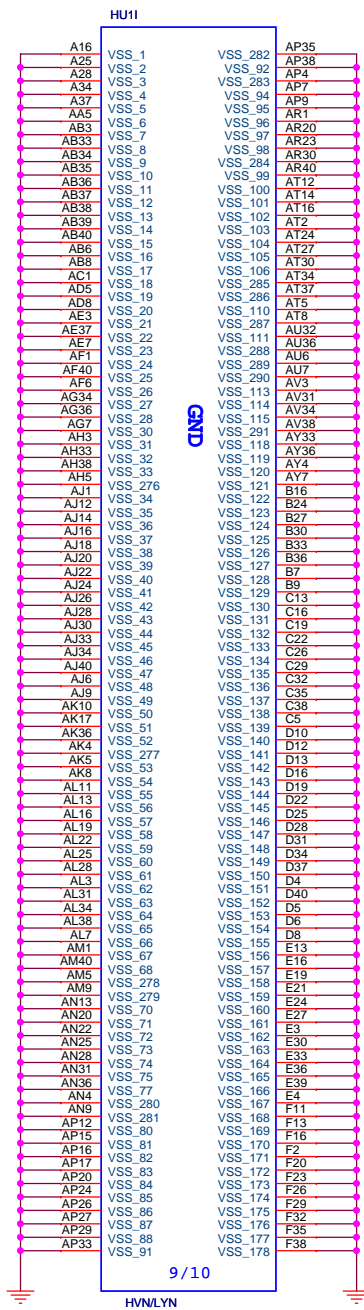
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Signals Not Used by the Lynnfield Processor, Listed by Platform

Platform	Interface	Signals Not Used ¹
Desktop, Server and Workstation Ixex Peak Platforms	Intel Flexible Display Interface	FDI_FSYNC[1:0]
		FDI_LSYNC[1:0]
		FDI_INT
		FDI_TX[7:0]
		FDI_TX#[7:0]
	Integrated Graphics Core Power	GFX_DPRSLPVR
		GFX_IMON
		GFX_VID[6:0]
		GFX_VR_EN
		VAXG
Desktop Ixex Peak Platforms	Memory	SA_DM[7:0]
	Memory Interface: RDIMM Related	SB_DM[7:0]
		VCCPWRGOOD_1
		SA_CS#[7:4]
		SB_CS#[7:4]

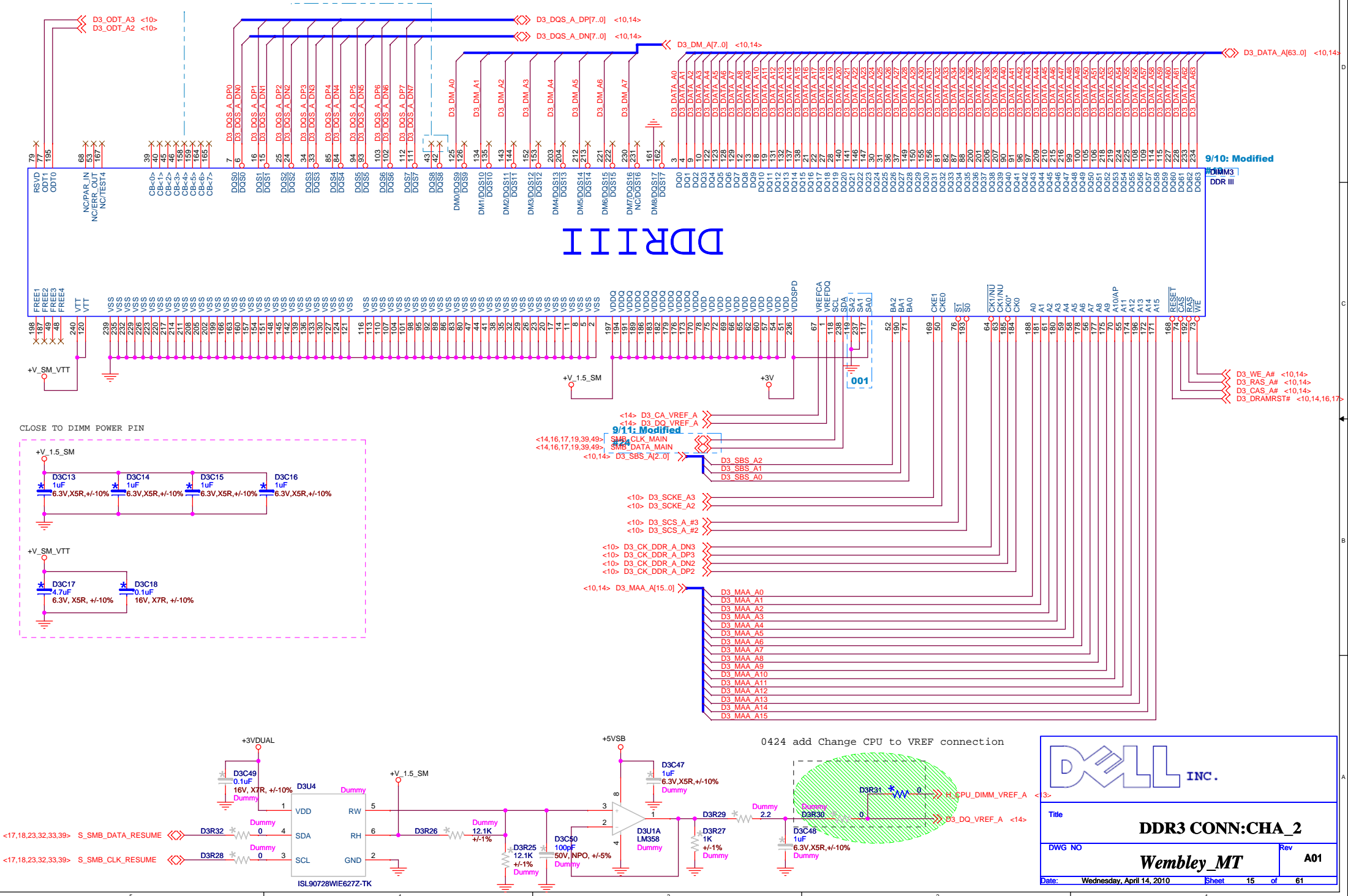




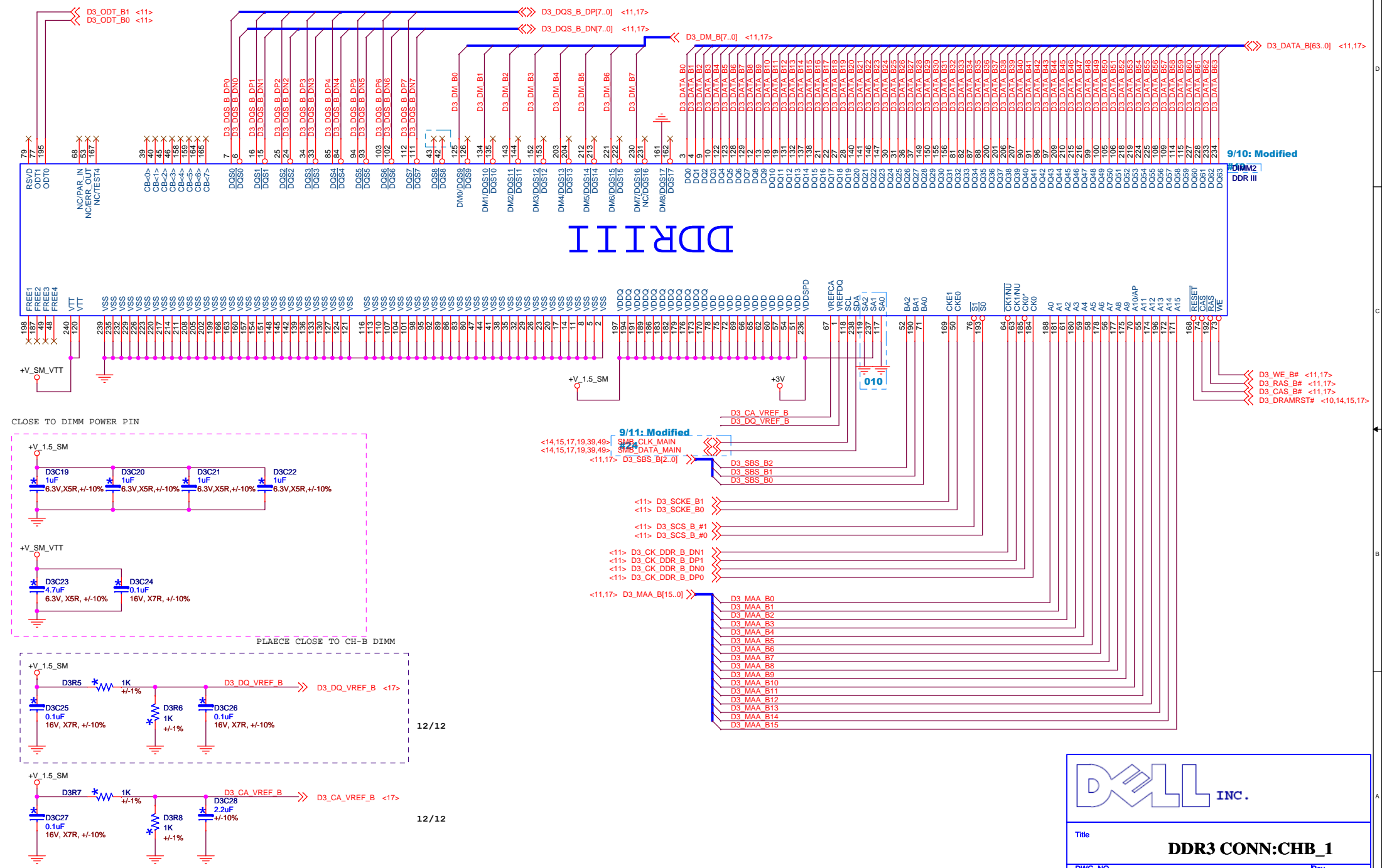
由于Power要follow CRB 下述测试点不能加上：
HTP59, HTP50, HTP52, HTP28, HTP49, HTP62, HTP23, HTP64, HTP63

Title	
CPU-7:GND	
DWG NO	Rev
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CHANNEL A BANK 2
SMB ADDRESS:001

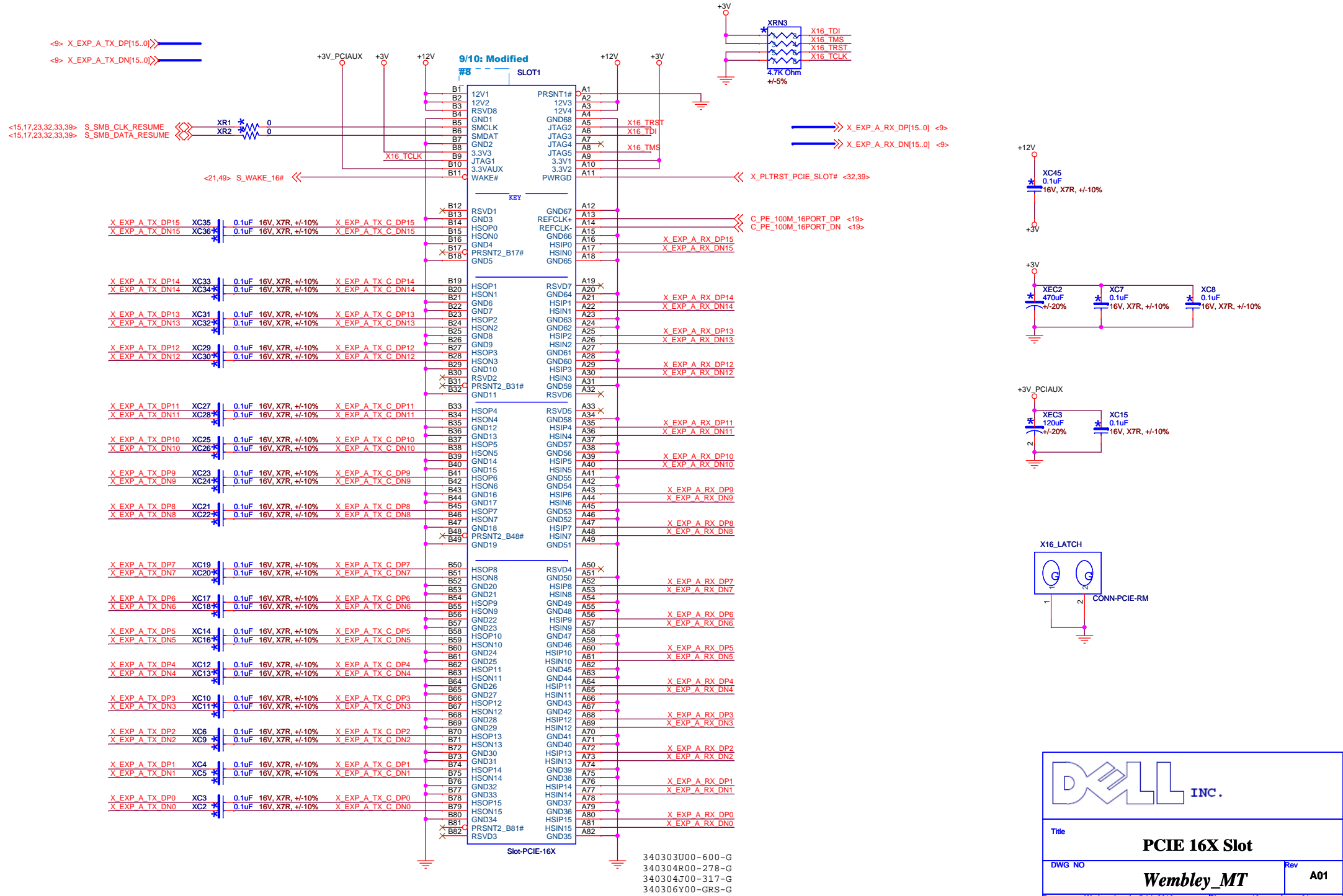



CHANNEL B BANK 1
SMB ADDRESS:010



Title		
DDR3 CONN:CHB_1		
DWG NO	Rev	A01
Wembley_MT		
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PCIEX16





INC.

Title

PCIE 16X Slot

DWG NO

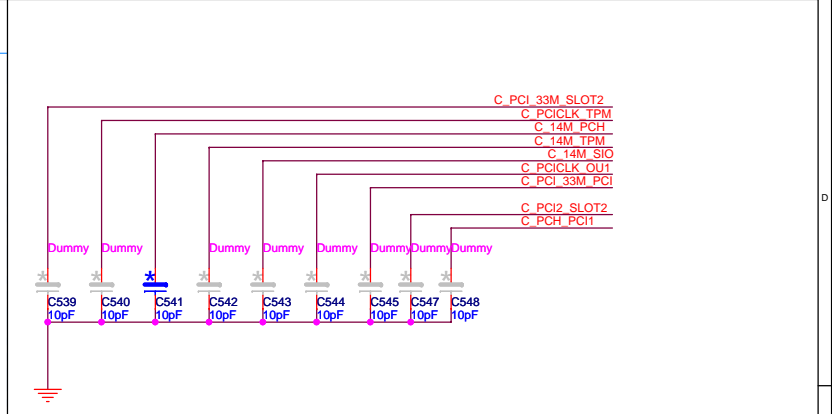
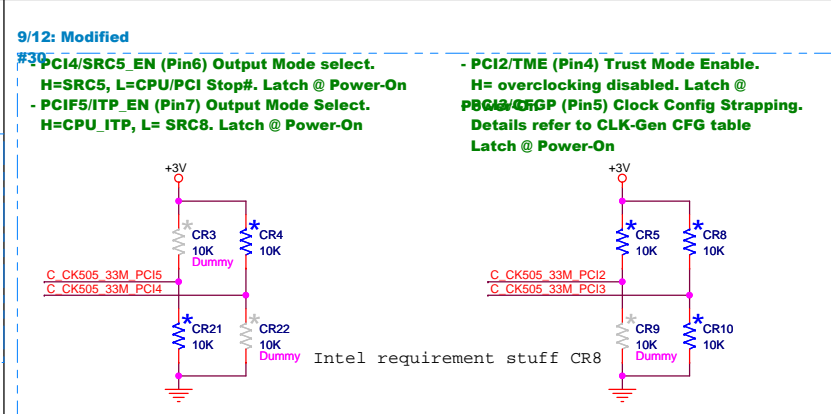
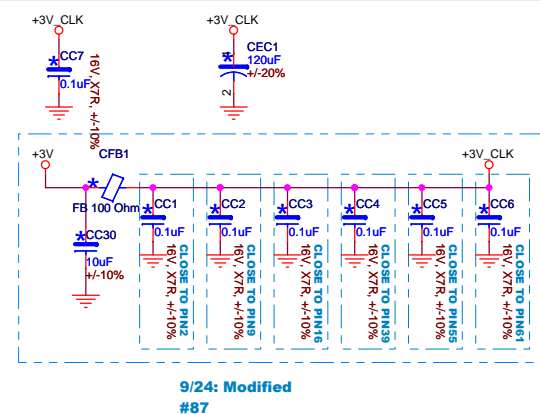
Wembley_MT

Date: Wednesday, April 14, 2010

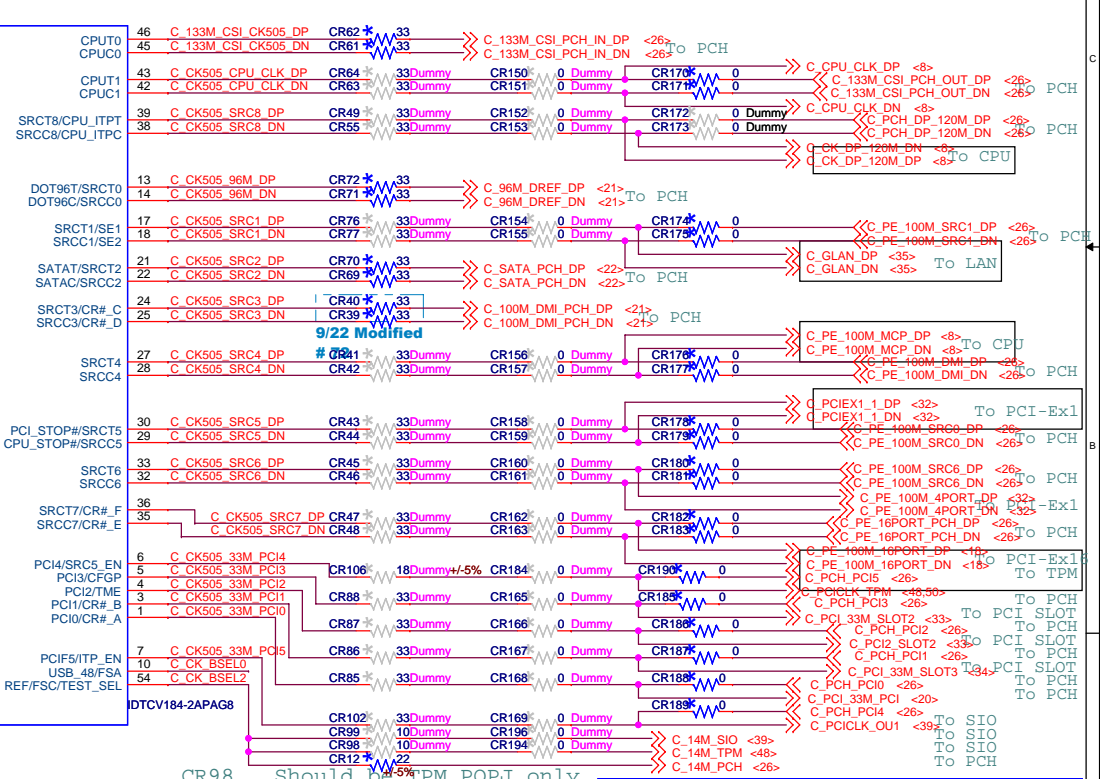
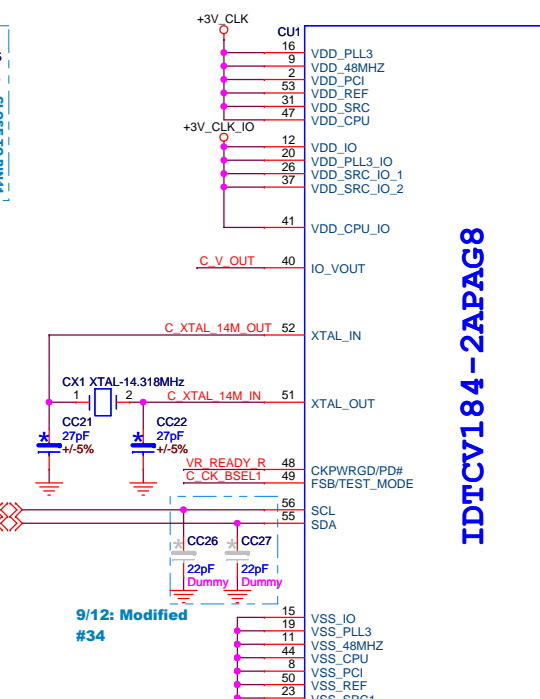
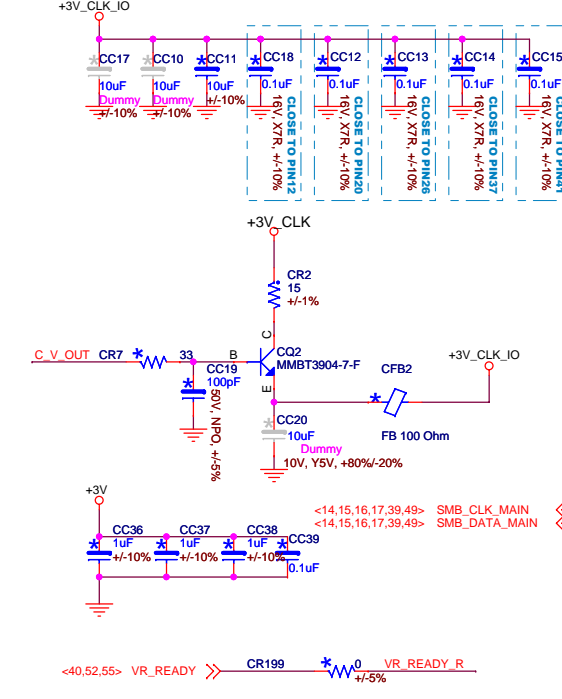
Sheet 18 of 61

Rev

A01

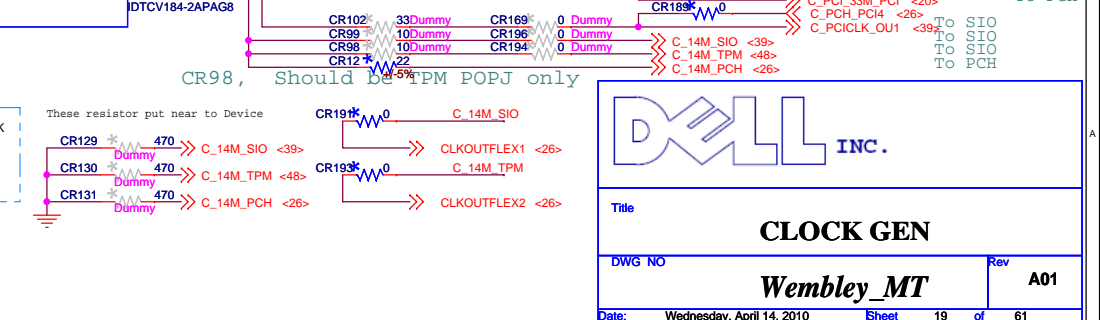
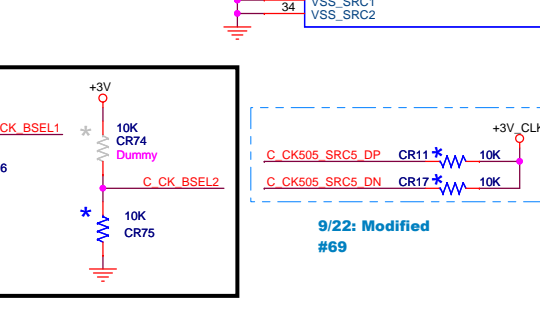


+3V_CLK_IO



9/11: Modified #27
check sequencing of CLK & Vcore, once DG come out

FREQ	BSEL0	BSEL1	BSEL2
100	1	0	1
133	1	0	0

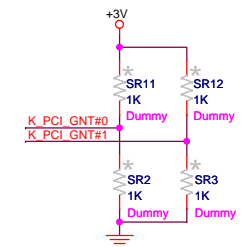
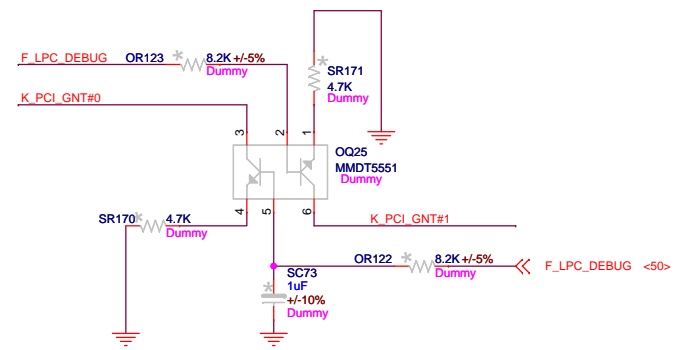
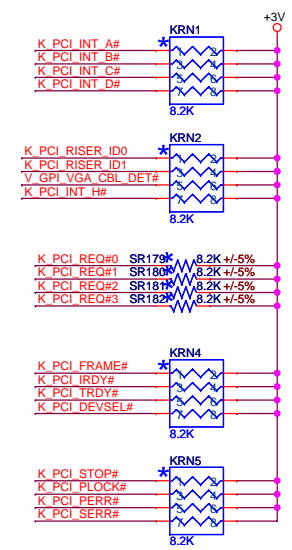
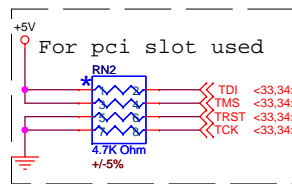
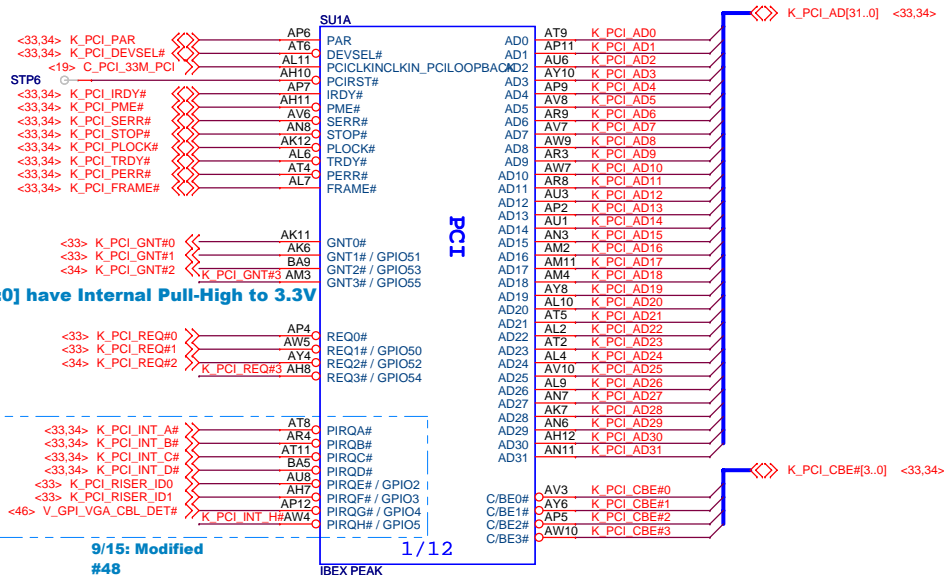


DELL INC.

CLOCK GEN

DWG NO: **Wembley_MT**

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Boot BIOS Select

Boot Device	GNT1	GNT0
LPC	0	0
PCI	1	0
Reserved	0	1
SPI	1	1

EDS 1.0 / DG 0.8
GNT2 configures DMI for ESI compatible mode is for server platforms only

K_PCI_GNT#2 SR4 1K
 K_PCI_GNT#3 SR1 1K
GNT3# Internal pull-up.

EDS 1.0 / DG 0.8
GNT3 is Swap OverRide Strap
OverRide if sample Low

Title

PCH-1:PCI

DWG NO

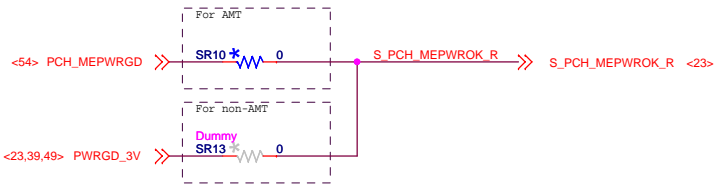
Wembley_MT

Date: Wednesday, April 14, 2010

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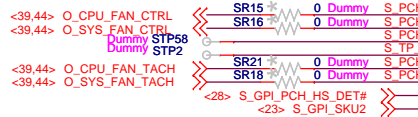
Rev

A01

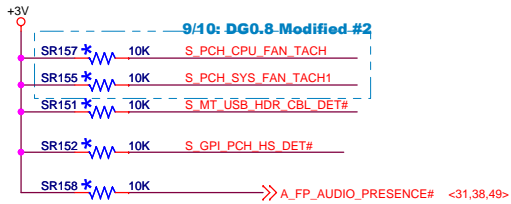
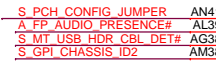


STEVEN UPDATE 08/09/01

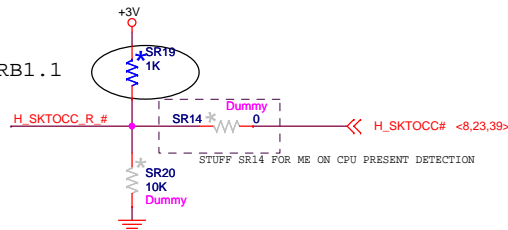
Place close to FAN conn



SMSC 5524 doesn't support SST



Follow CRB1.1



CLINK

FAN

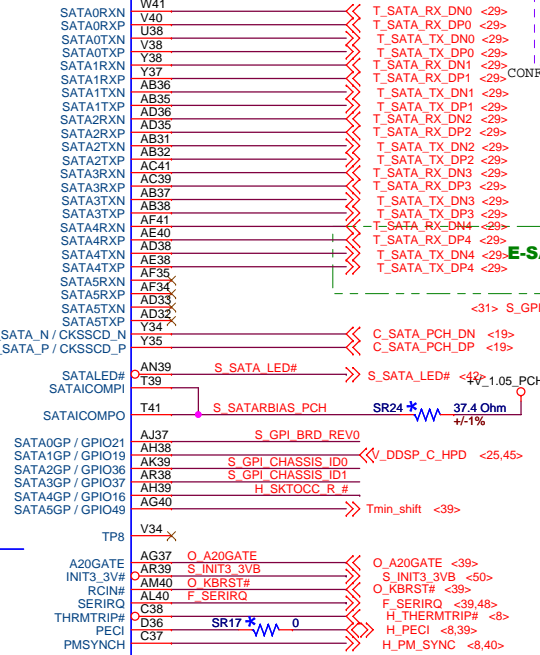
GPIO

SATA

HOST

3/12

IBEX PEAK



CONFIGURABLE CPU OUTPUT STRONGER IF LOW

E-SATA

<31> S_GPI_CHASSIS_ID2

<4> V_1.05_PCH

<39> S_GPI_BRD_REV0

<39> S_GPI_CHASSIS_ID0

<39> S_GPI_CHASSIS_ID1

<39> S_GPI_CHASSIS_ID2

<39> S_GPI_PCH_HS_DET#

<39> S_GPI_BRD_REV1

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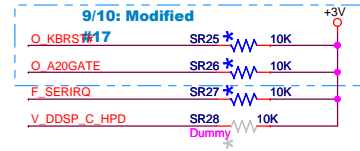
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<39> S_GPI_BRD_REV0

<39> S_GPI_BRD_REV1

<39> S_GPI_BRD_REV0

<39> S_GPI_BRD_REV1



SR154 (unstuff)change to SR143 (stuff) 0407

Chassis ID

ID2	ID1	ID0	Type
1	0	1	SFF(Mr. Big)
1	0	0	DT(Motley Crue)
0	0	0	MT(Bon Jovi)
0	1	1	Wenger

BOARD ID

Rev1	Rev0	Type
0	0	Default
0	1	Reserved
1	0	Reserved
1	1	Reserved

PCH_CONFIG

Need to check

S_PCH_CONFIG_JUMPER



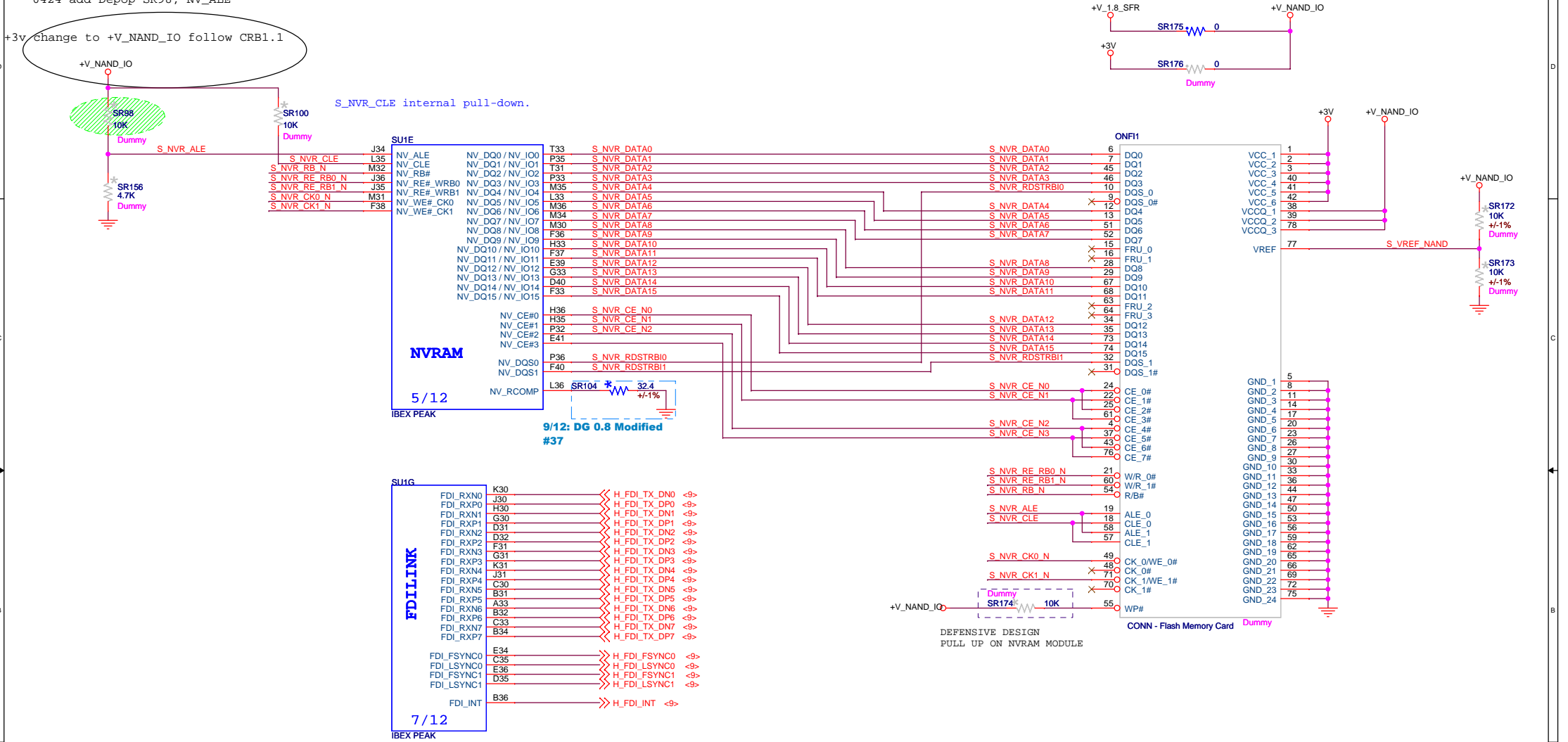
Title: PCH-3:SATA/HOST/FAN

DWG NO: Wembley_MT Rev: A01

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0424 add Depop SR98, NV_ALE

+3v change to +V_NAND_IO follow CRB1.1

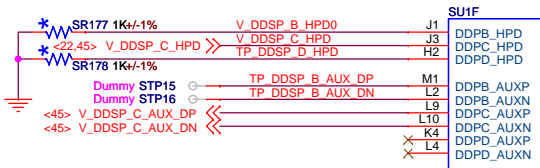


Title
PCH-5:NVRAM/FDI

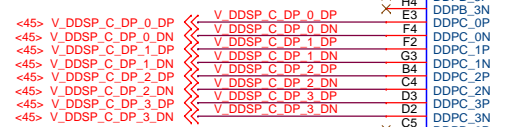
DWG NO
Wembley_MT

Date: Wednesday, April 14, 2010 Sheet 24 of 61

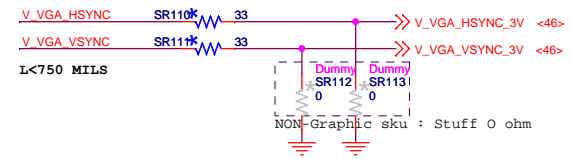
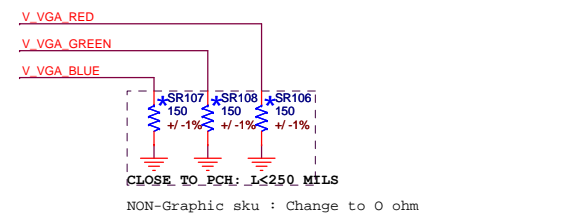
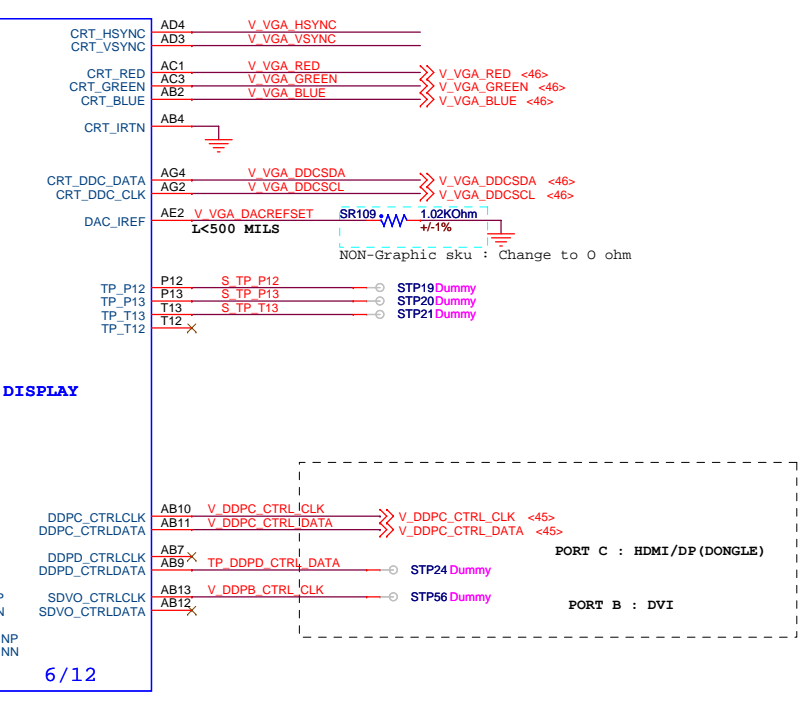
HPD needs be grounded on unused(ground via 1k resistor).
Follow Design Guide 1.0

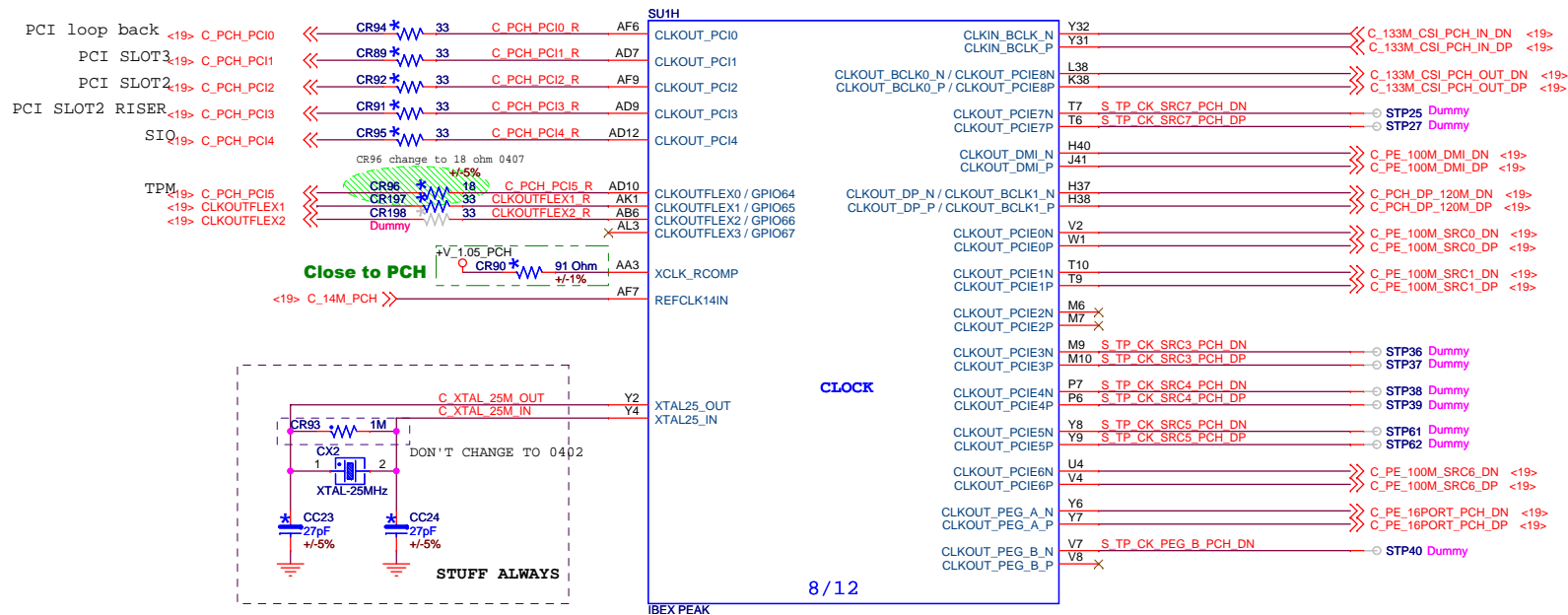


PORT B : Capable of SDVO/HDMI/DVI/DP



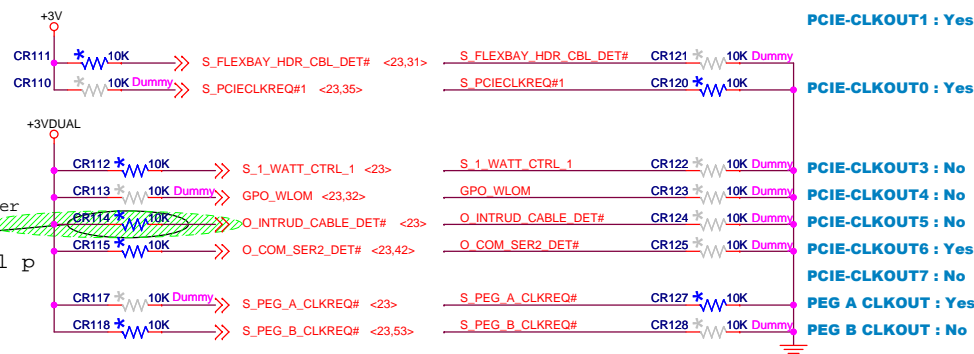
PORT C : Capable of DP/HDMI/DVI






0424 add for DELL tracker

B0 stepping will have internal pull up to 1.05V on GPIO44

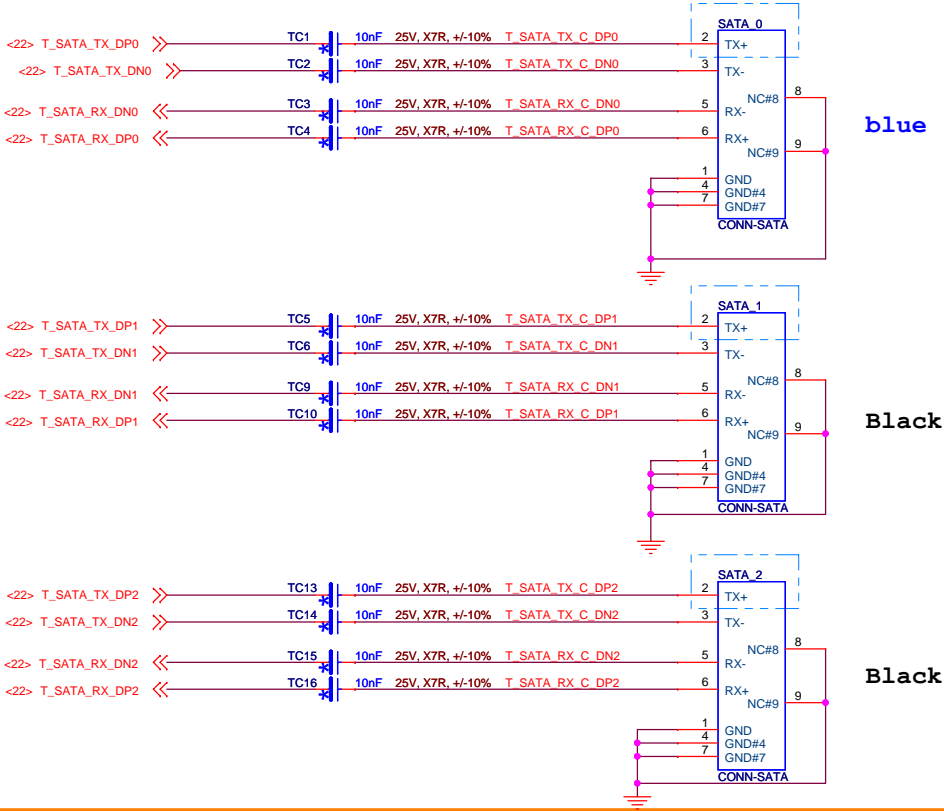


9/11: CRB 1.0
Modified #20

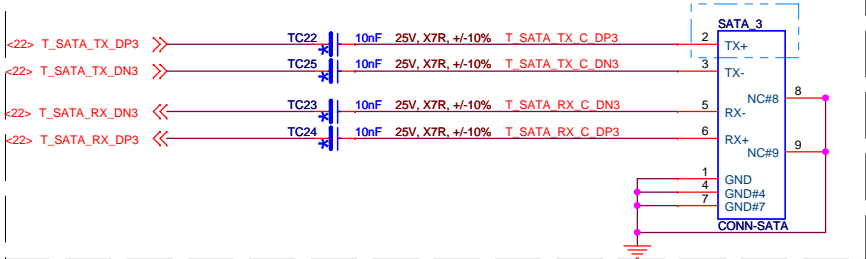
		
Title		
PCH-8:CLOCK		
DWG NO	Rev	A01
Wembley_MT		
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SATA x 3

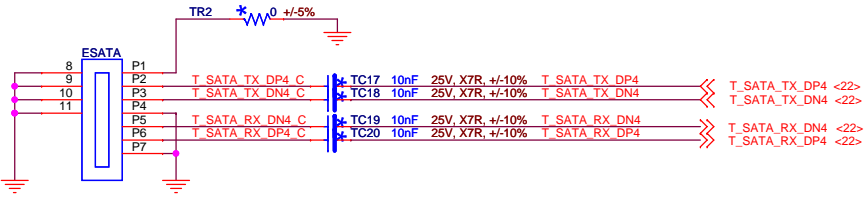
Need to Sub Connector Color



SATA port 3 only for MT Black



E SATA



Title

SATAx3 / eSATA

DWG NO

Wembley_MT

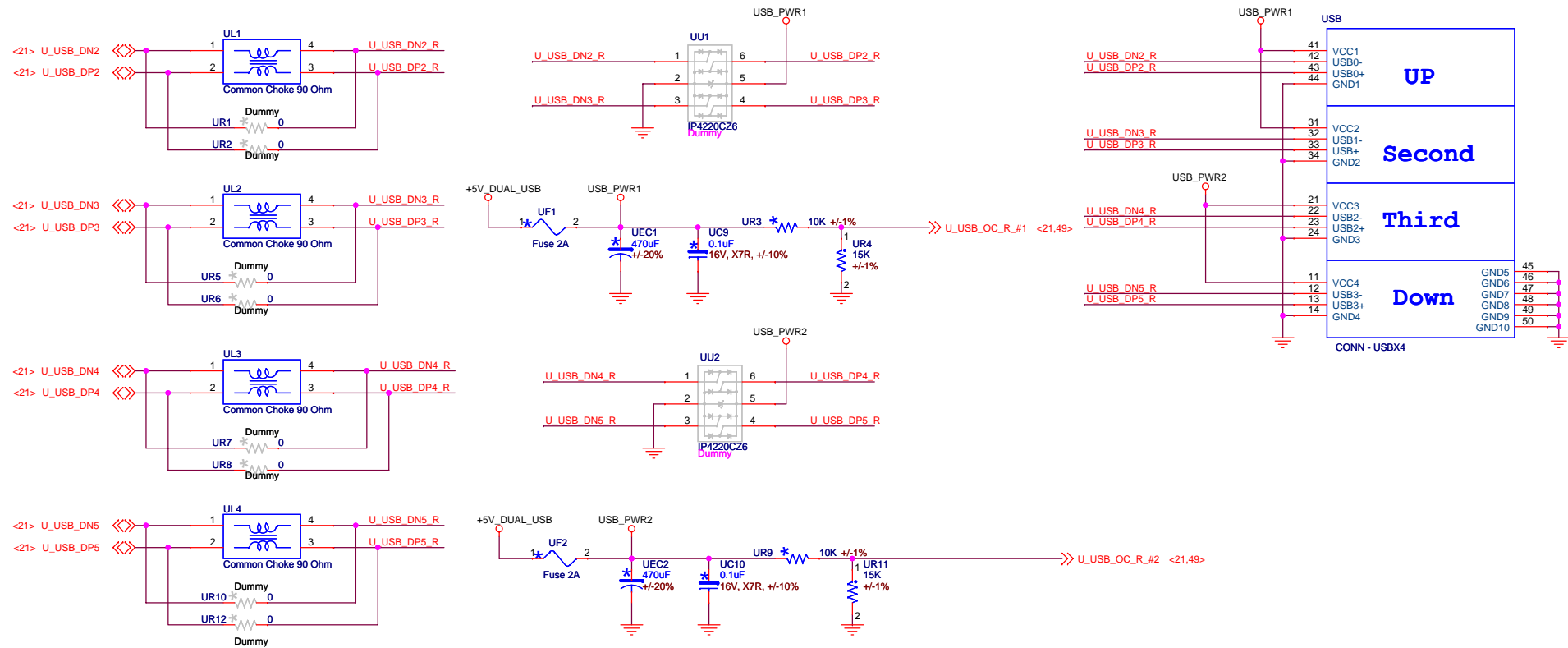
Date: Wednesday, April 14, 2010

Rev

A01

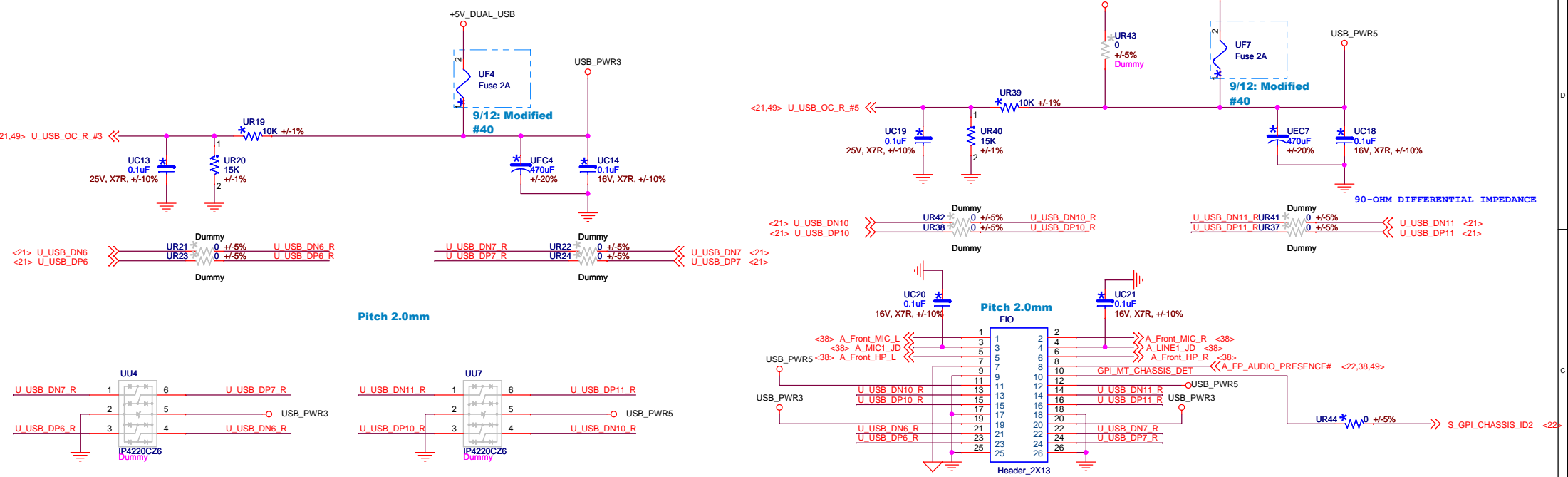
Sheet 29 of 61

Rear USB CONNECTOR

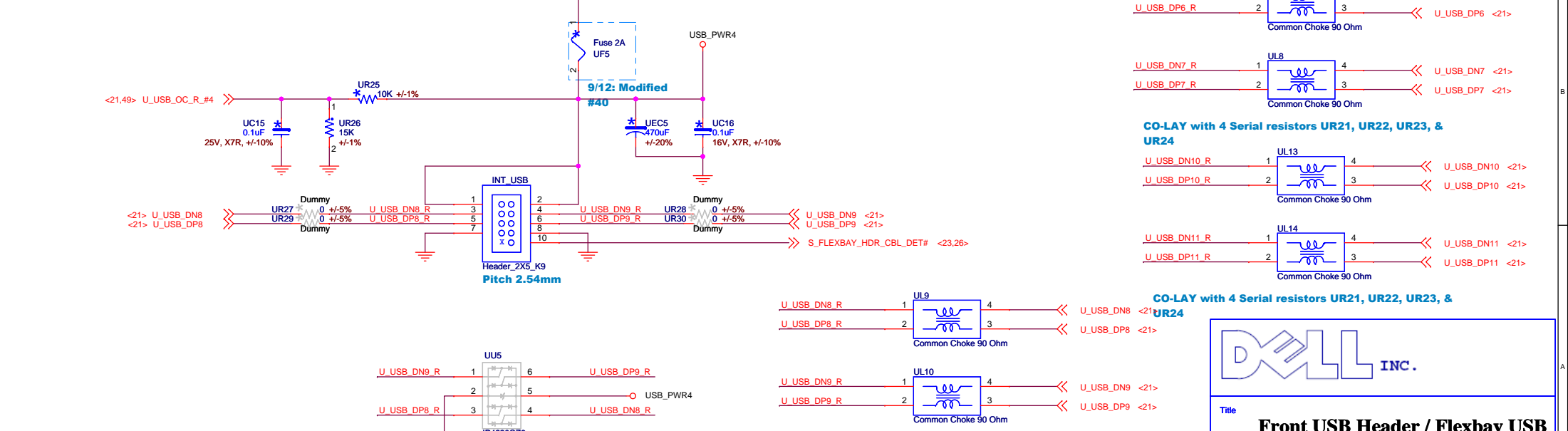


Title		
Rear USB		
DWG NO	Wembley_MT	Rev A01
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Front USB Header



FLEXBAY



Title

Front USB Header / Flexbay USB

DWG NO

Wembley_MT

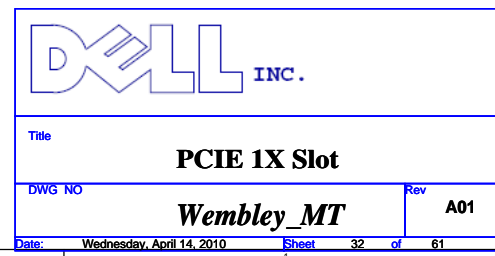
Rev

A01

Date: Wednesday, April 14, 2010

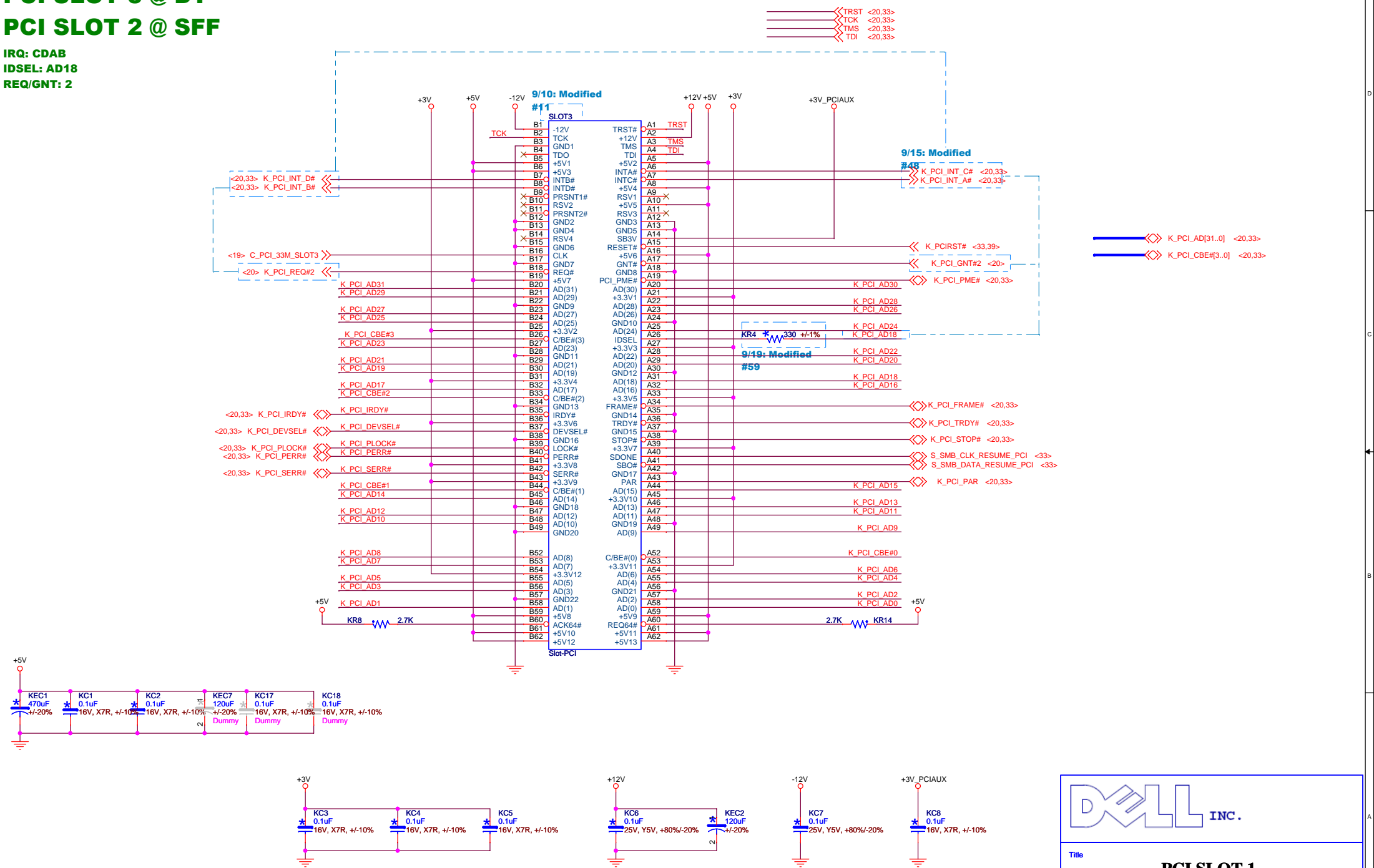
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PCIE X1 SLOT @ DT/SFF/MT



PCI SLOT 3 @ DT
PCI SLOT 2 @ SFF

IRQ: CDAB
IDSEL: AD18
REQ/GNT: 2



Title

PCI SLOT 1

DWG NO

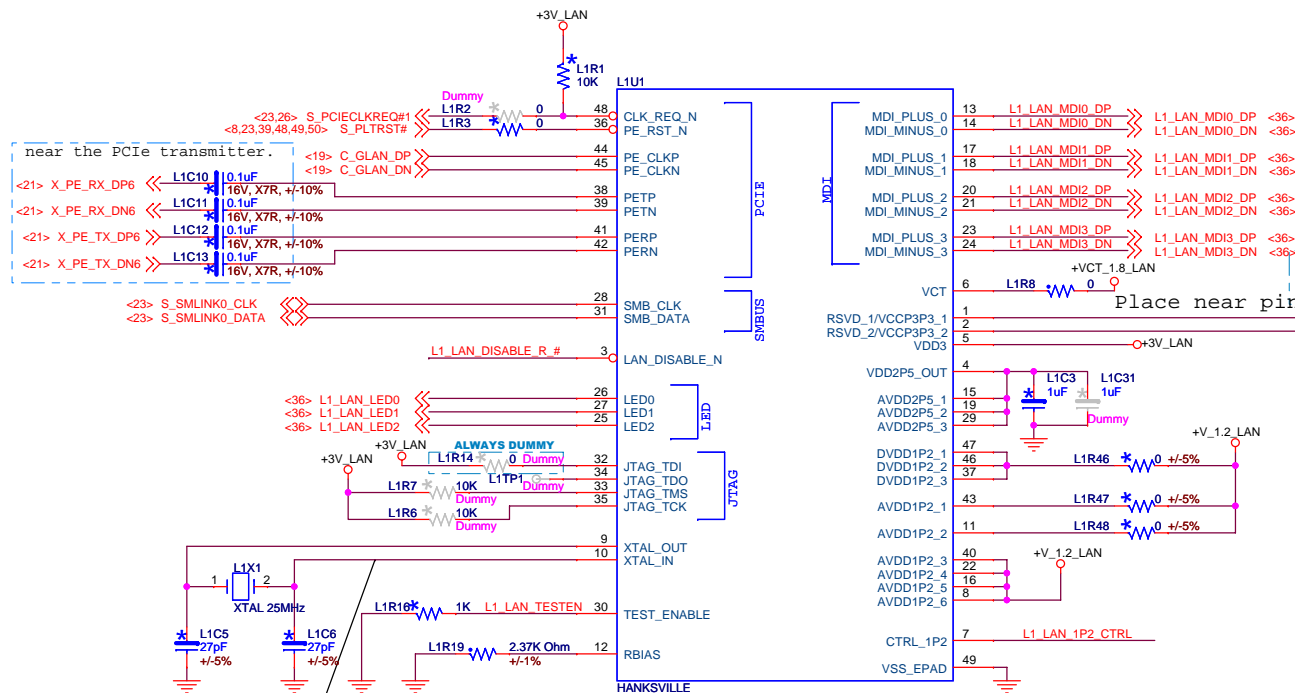
Wembley_MT

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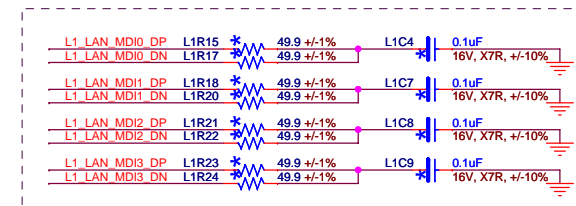
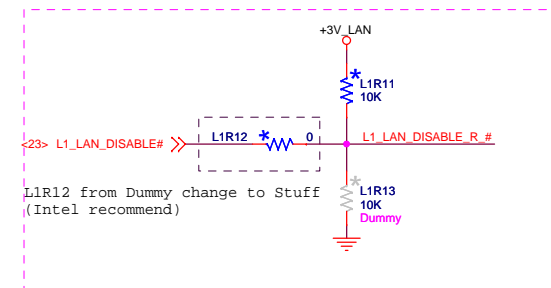
Rev

A01



less than 325 mils

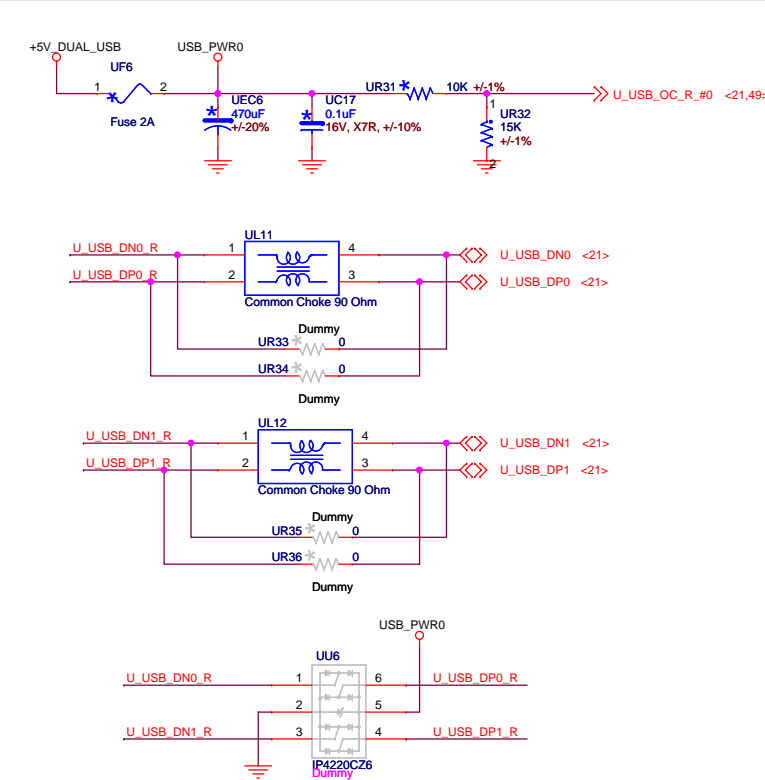
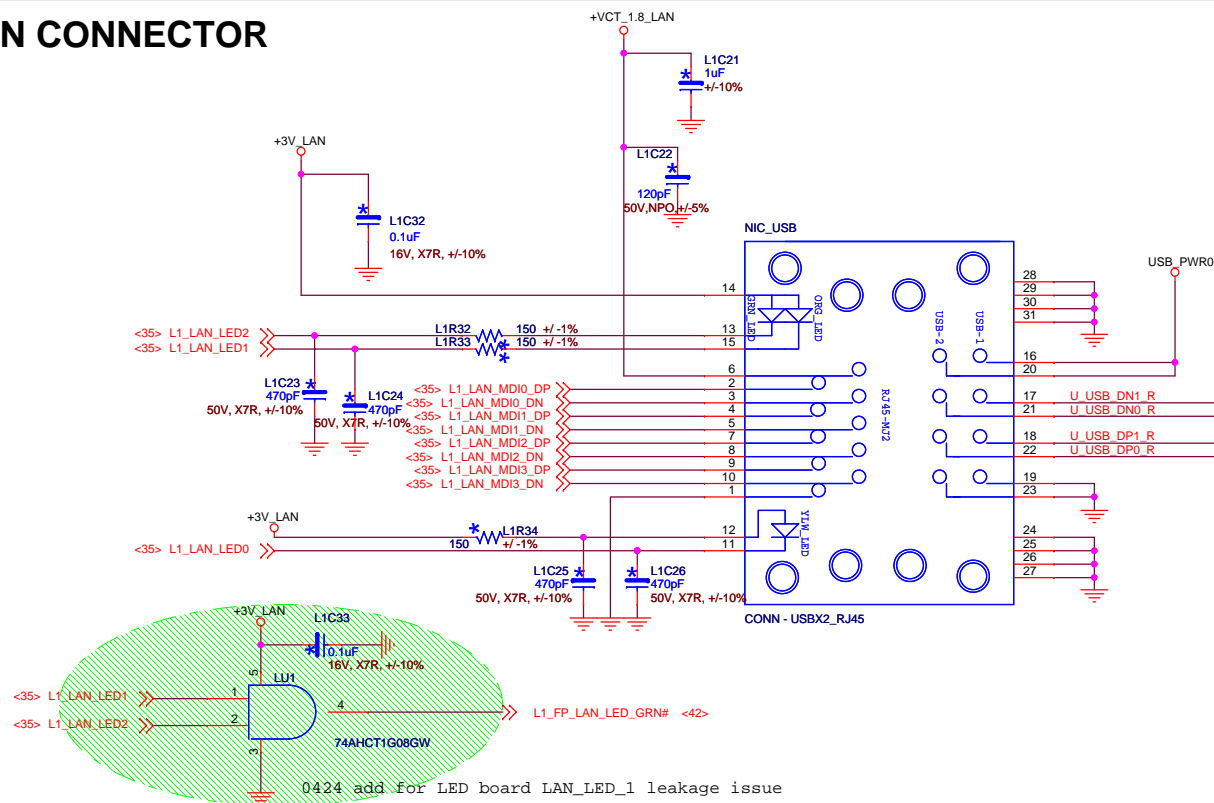
9/16: 82578 GbE PHY Datasheet 0.9:
Modified #54
Need Double
Check
Different with 9.3



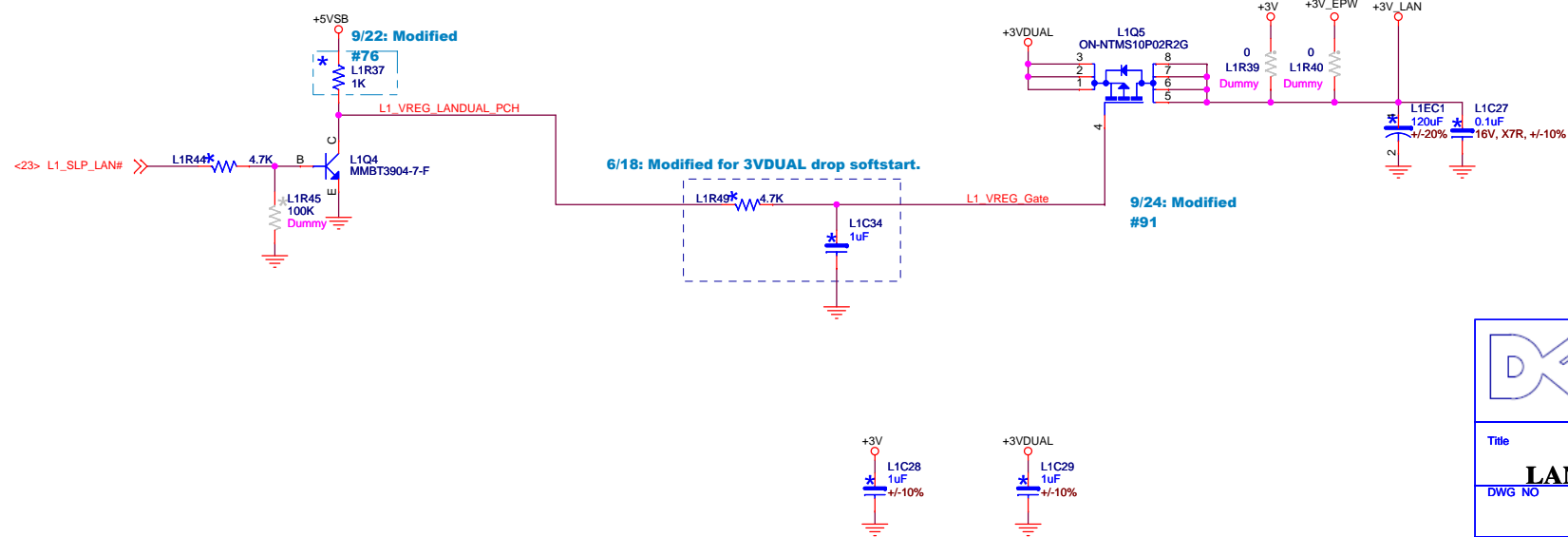
CLOSE TO PHY

DELL INC.	
Title	
LAN:INTEL HANKSVILLE	
DWG NO	Rev
Wembley_MT	A01
Date: Wednesday, April 14, 2010	Sheet 35 of 61

LAN CONNECTOR



LAN POWER



Title

LAN POWER & LAN/USB CONN

DWG NO

Wembley_MT

Rev

A01

Date

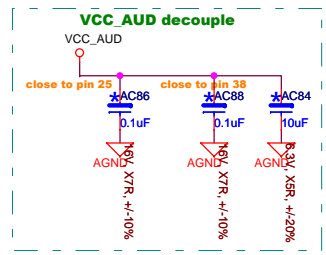
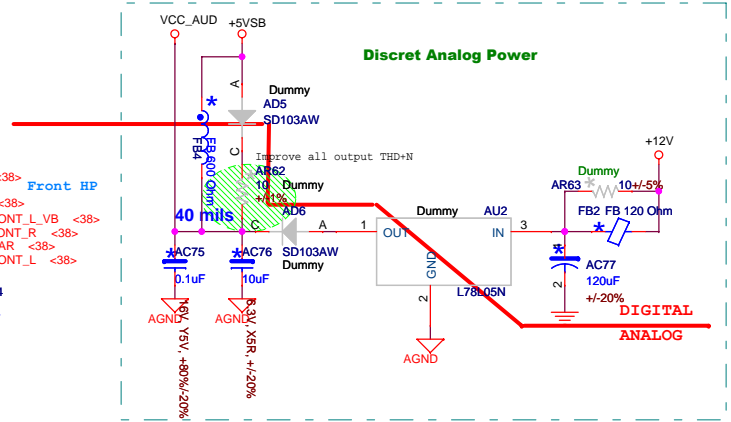
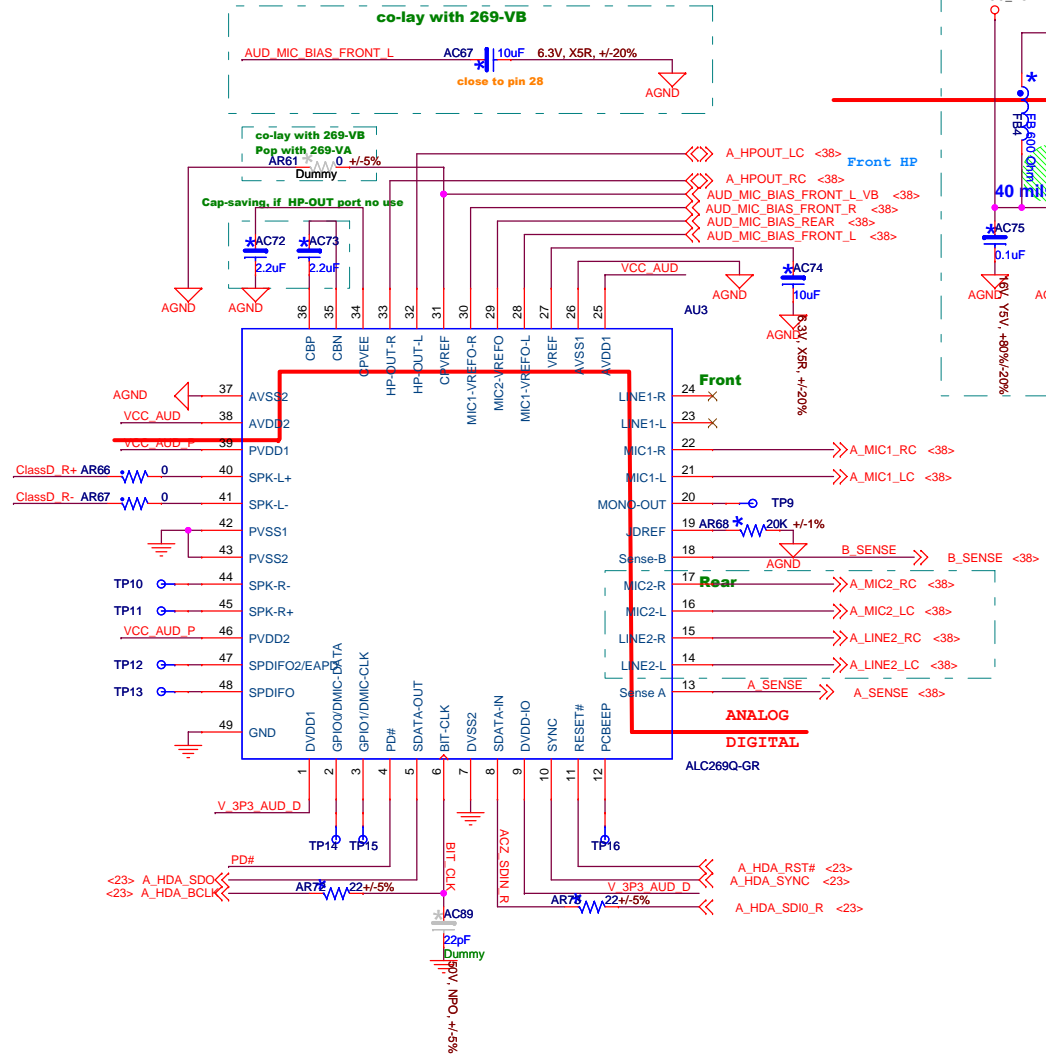
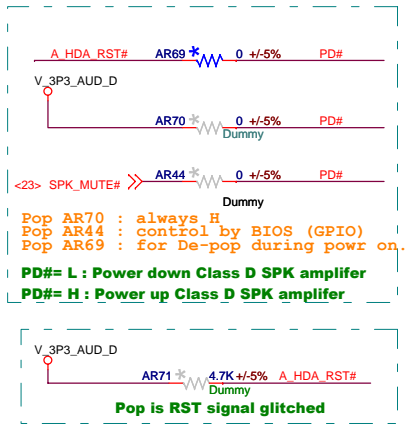
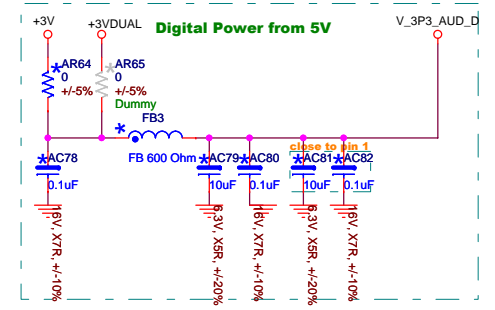
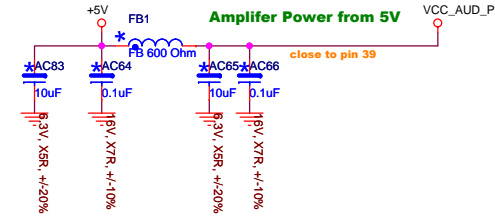
Wednesday, April 14, 2010

Sheet

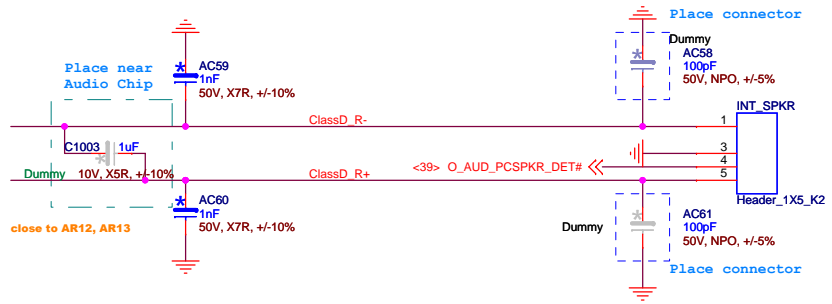
36

of

61



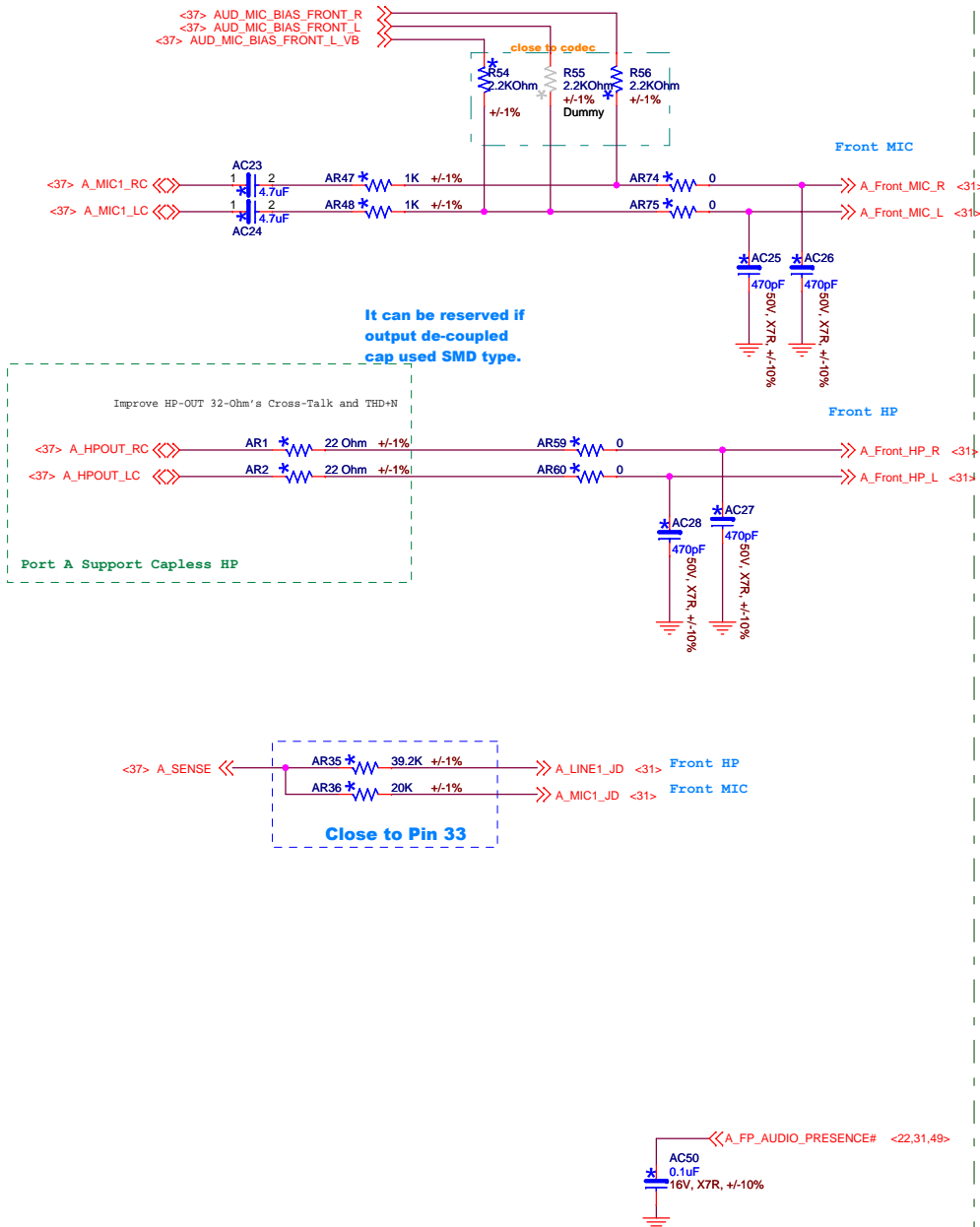
For ALC269-VB option
 Dummy AD5,AD6,AR61,AR62,AU2
 Stuff AC67 , FB4 (0ohm)
 Dymmy R55 , Stuff R54



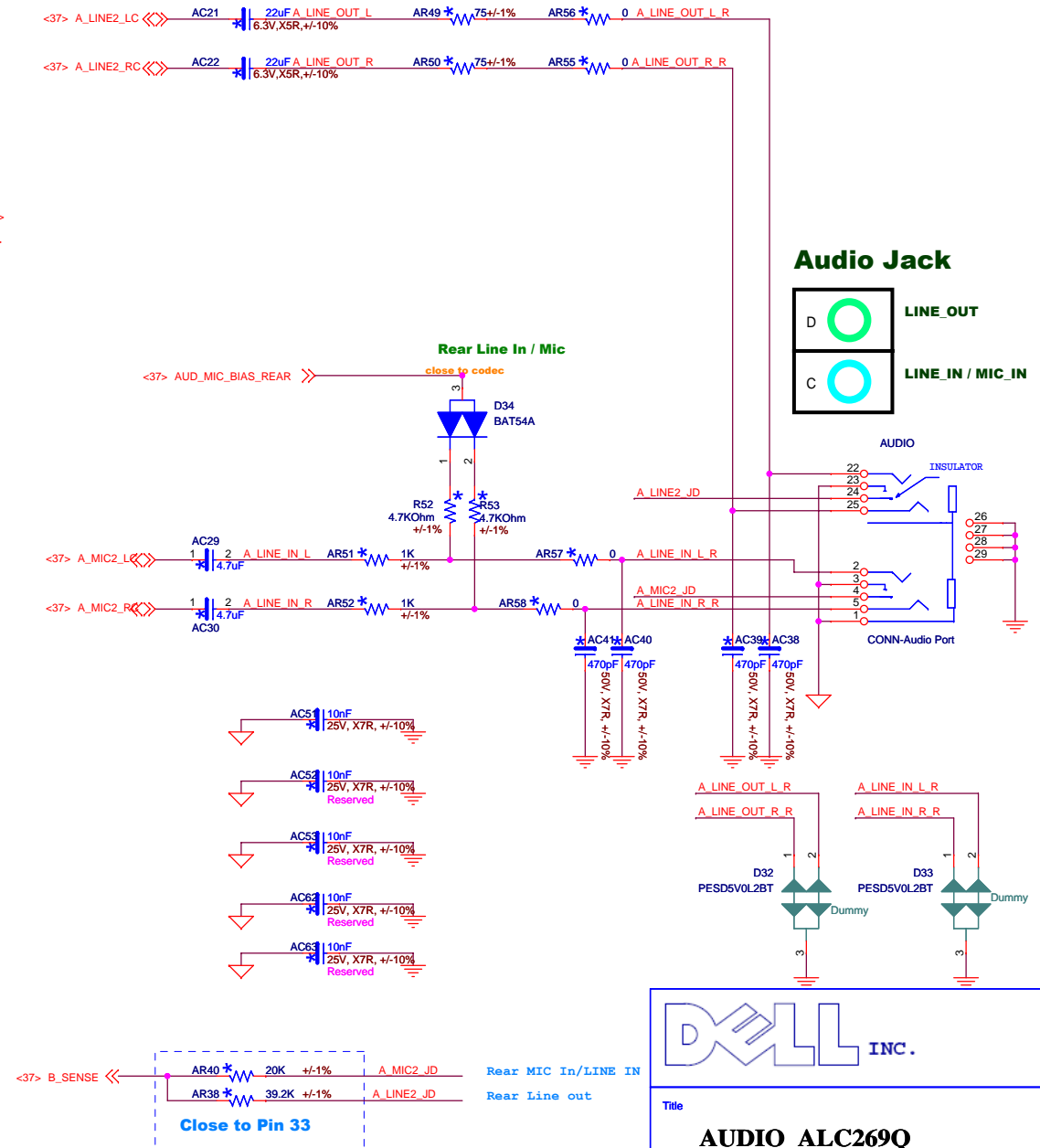
CHASSIS SPEAKER
 Header 1x5 cut2
 Pin.1--> Left-
 Pin.2--> NC key
 Pin.3--> GND
 Pin.4--> SPK det#
 Pin.5--> Left+

Title	
AUDIO ALC269Q	
DWG NO	Rev
Wembley_SFF	A01
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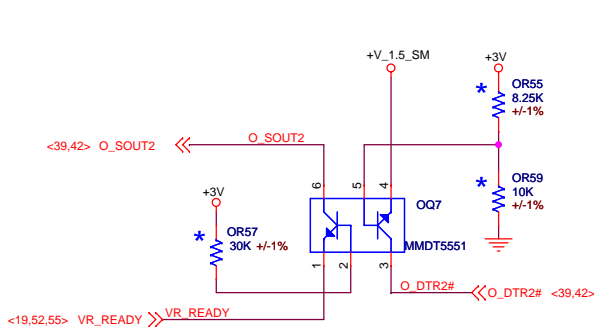
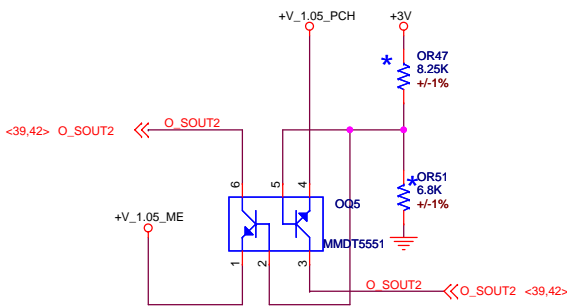
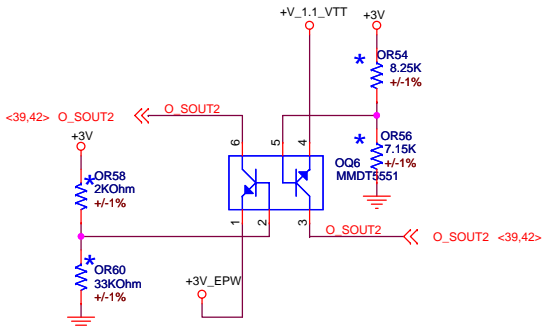
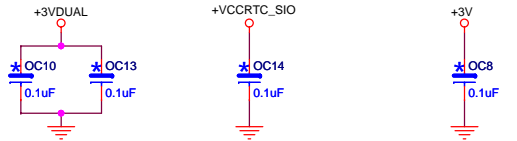
Front Audio



Rear Audio Jack



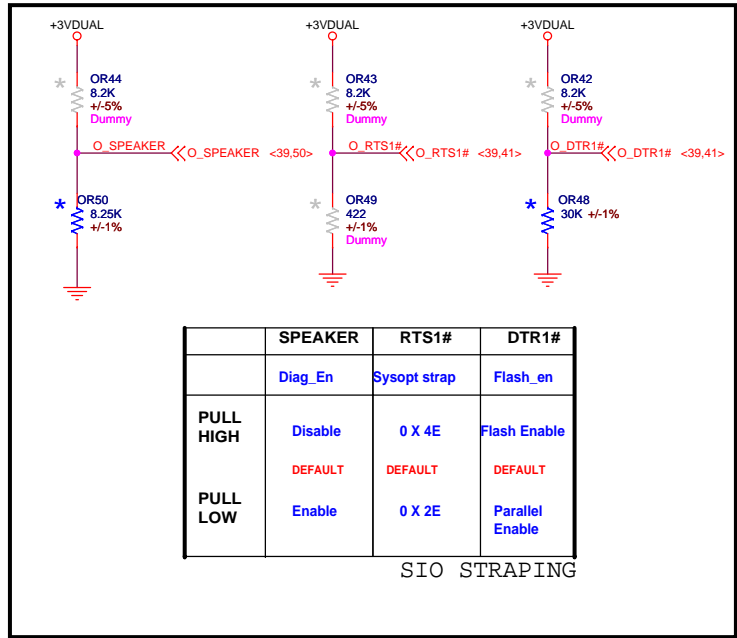
SCH5524 Decoupling



5524 PRE-POST DIAG PG GENERATION

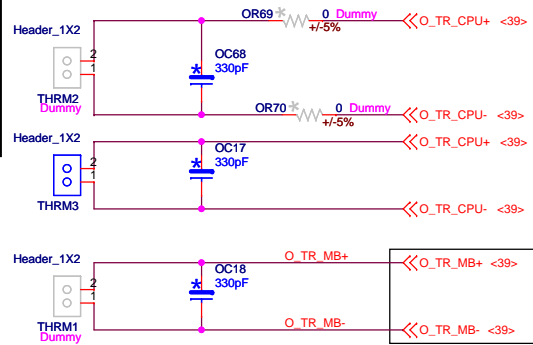
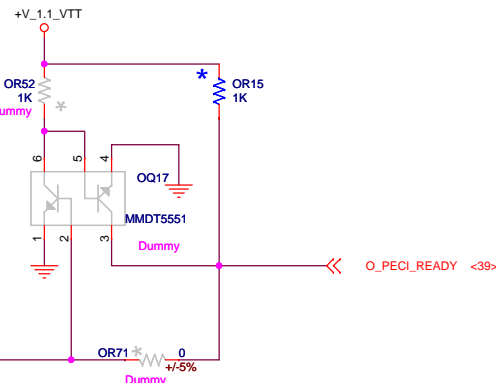
@5514
dummy all in this block

Only used For 5524



	SPEAKER	RTS1#	DTR1#
	Diag_En	Sysopt strap	Flash_en
PULL HIGH	Disable	0 X 4E	Flash Enable
PULL LOW	Enable	0 X 2E	Parallel Enable

SIO STRAPING



THERMAL SENSOR

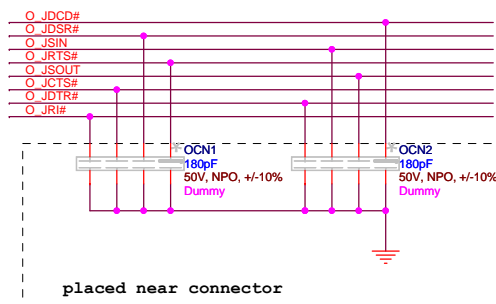
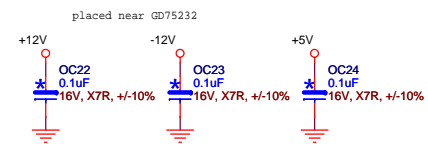
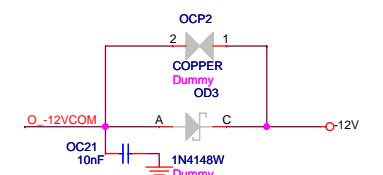
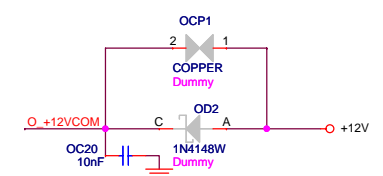
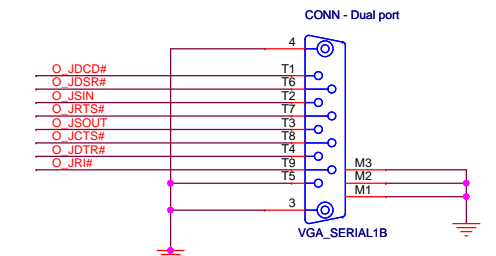
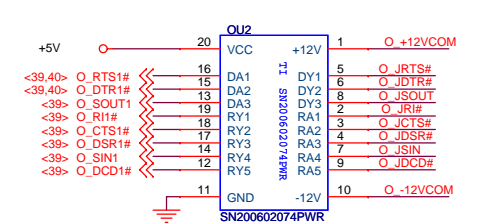


Title
SIO-SCH5544-2 (Misc)

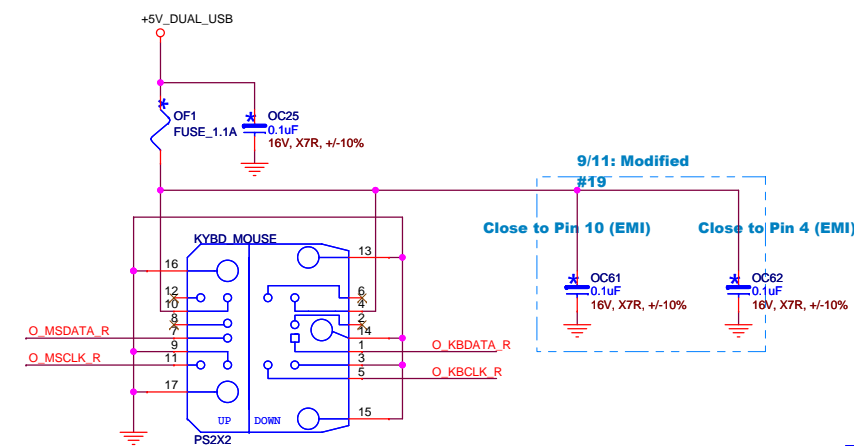
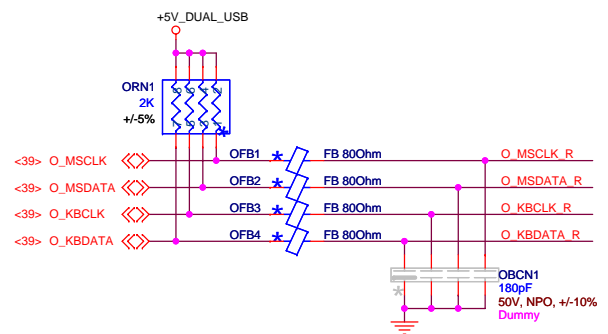
DWG NO
Wembley_MT

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COM Port



KB/MS



Title

COM Port / PS2

DWG NO

Wembley_MT

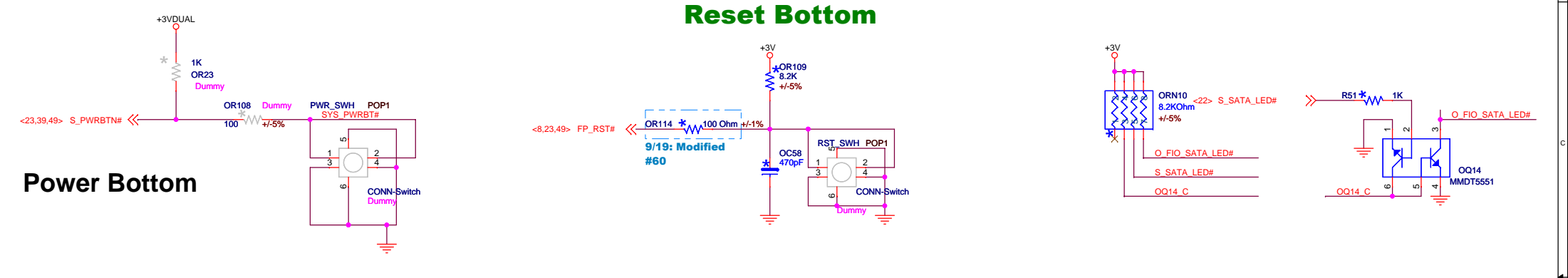
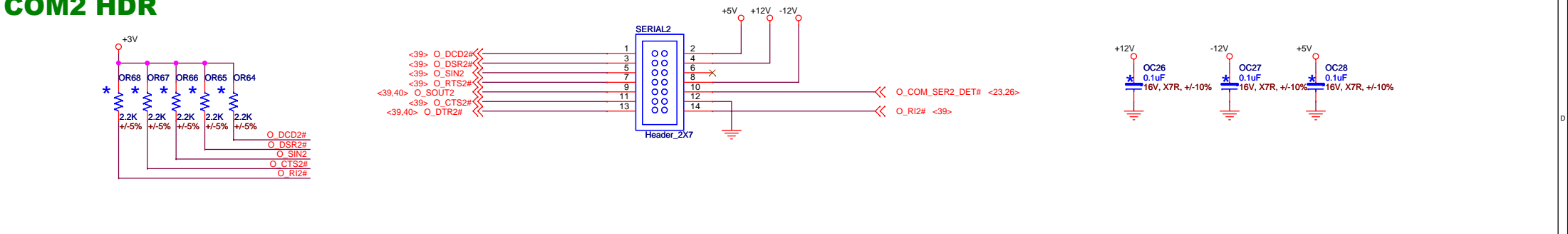
Date: Wednesday, April 14, 2010

Rev

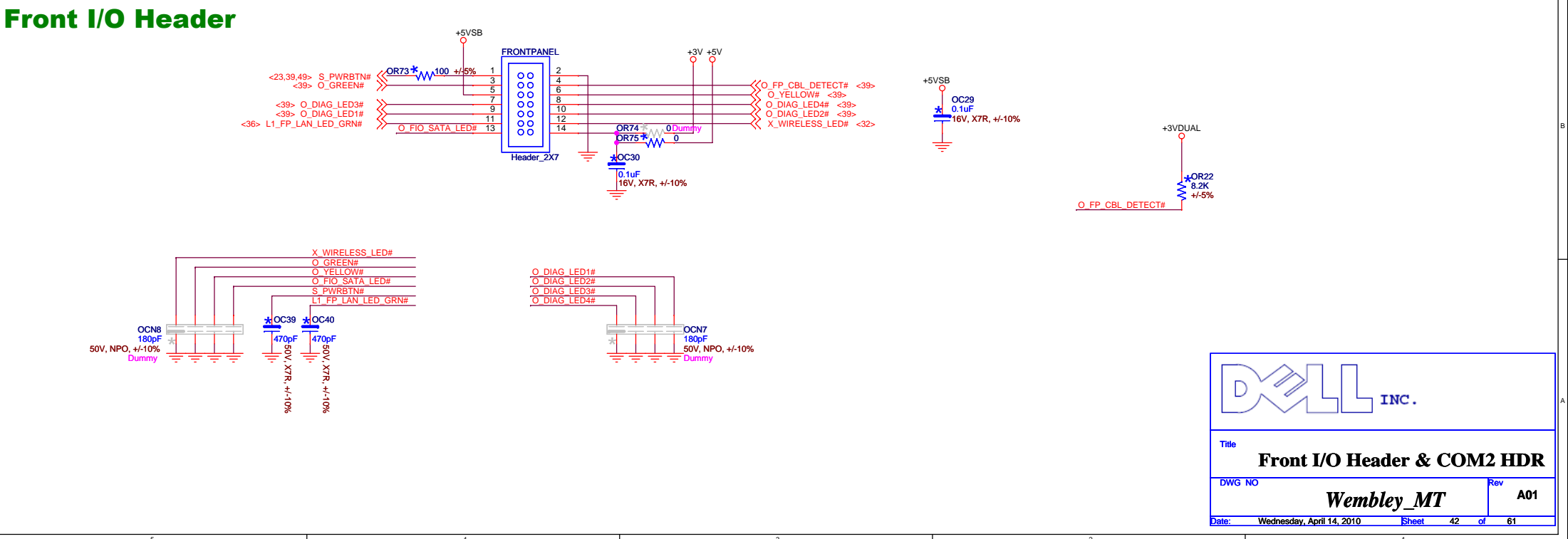
A01

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COM2 HDR



Front I/O Header



Title

Front I/O Header & COM2 HDR

DWG NO

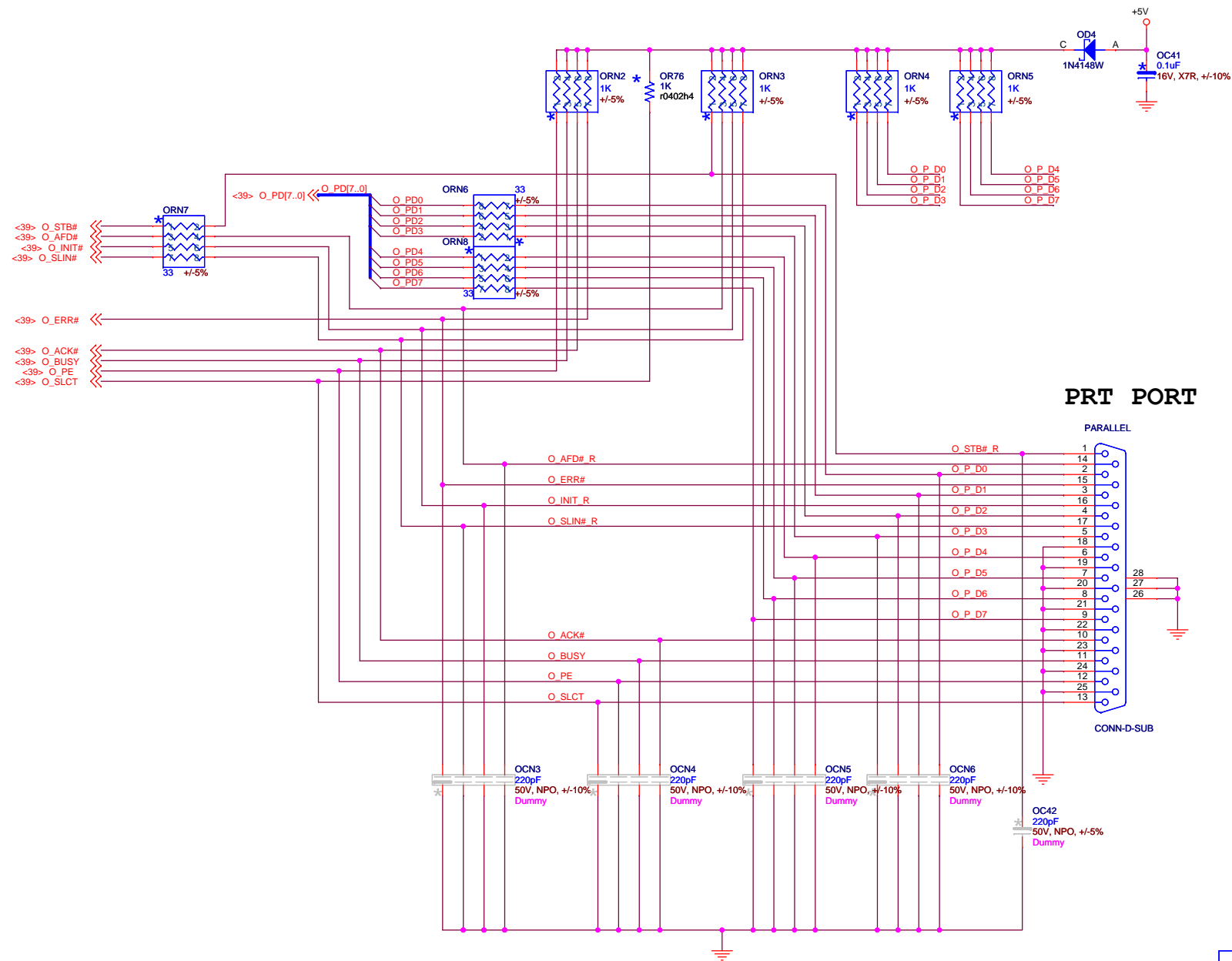
Wembley_MT

Rev

A01

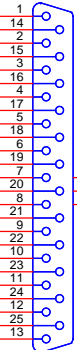
Date: Wednesday, April 14, 2010

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PRT PORT

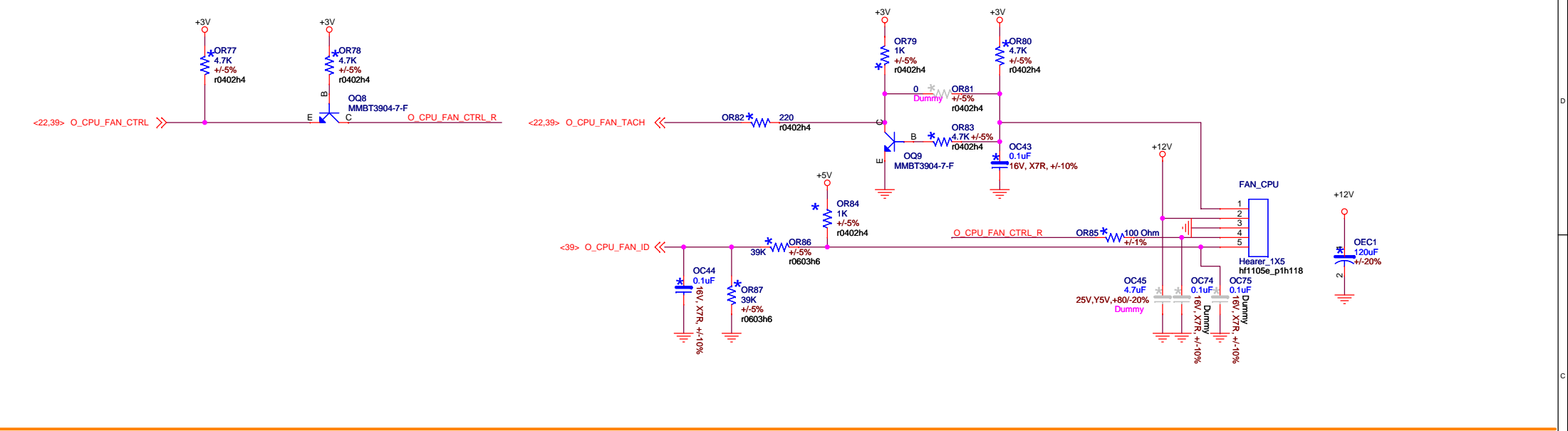
PARALLEL



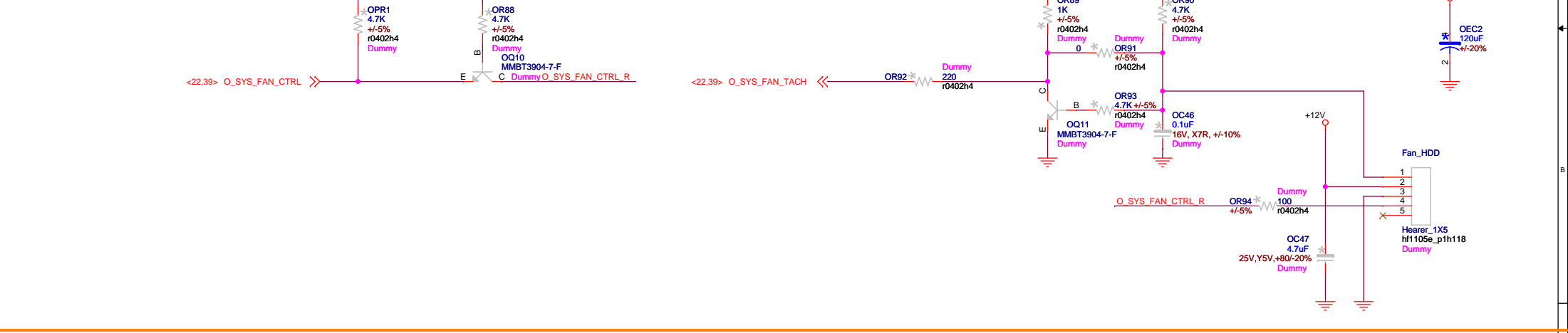
CONN-D-SUB

Title PRT PORT		
DWG NO Wembley_MT	Rev A01	
Date: Wednesday, April 14, 2010	Sheet 43	of 61

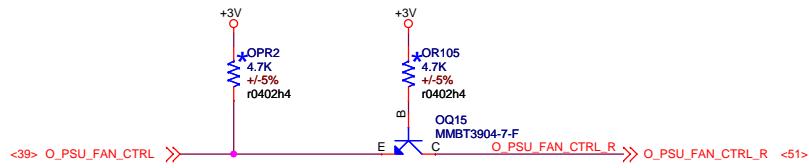
CPU Fan



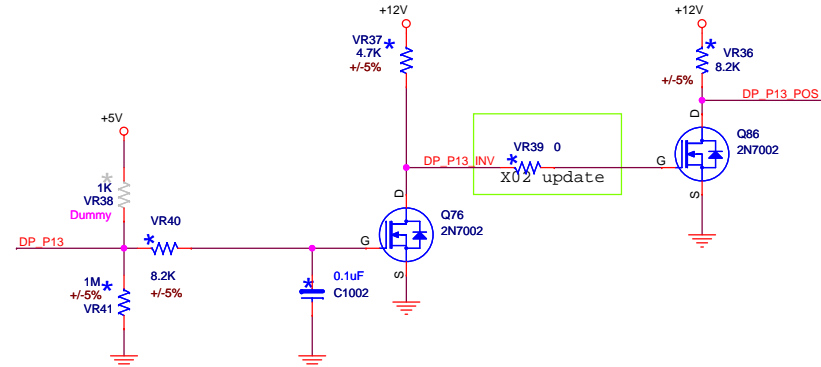
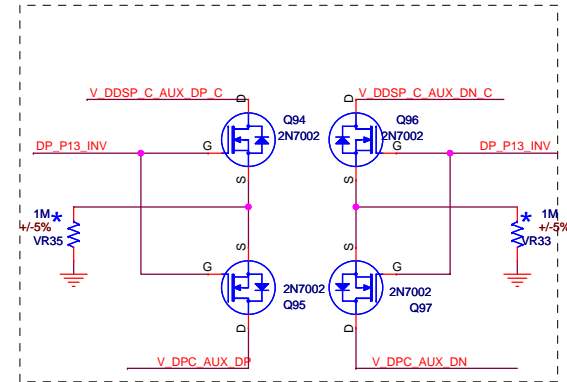
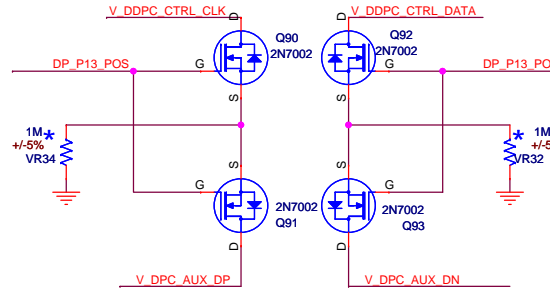
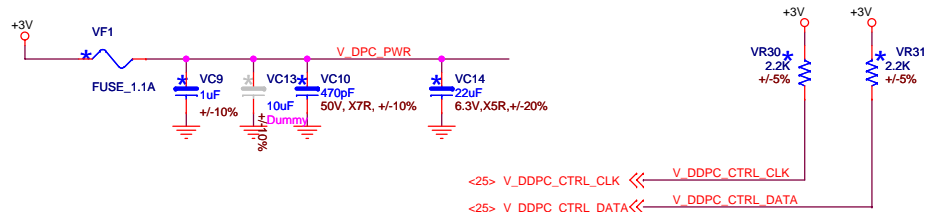
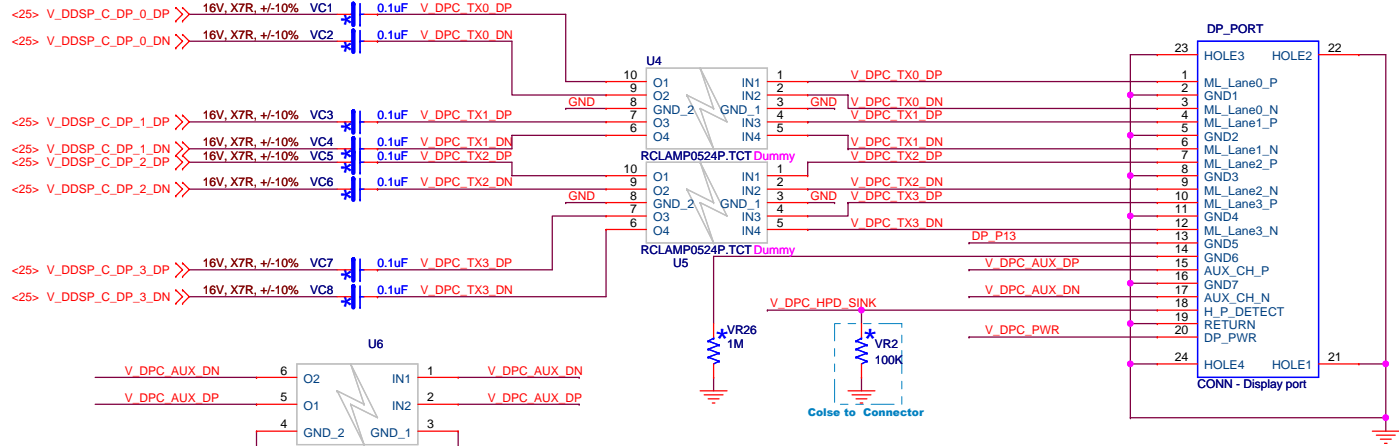
SYS Fan



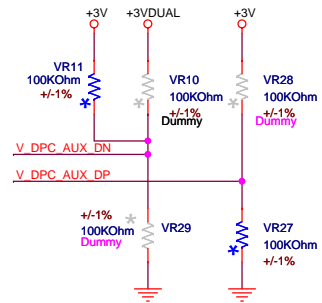
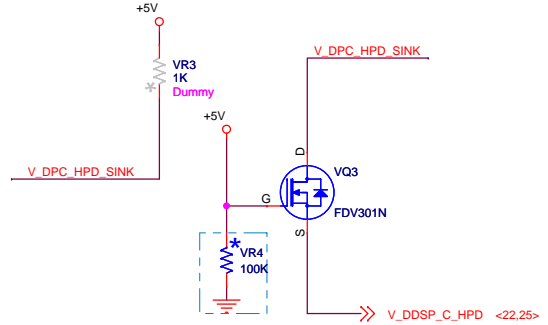
PSU Fan



Title		CPU & System FAN	
DWG NO		Rev	
Wembley_MT		A01	
Date:	Wednesday, April 14, 2010	Sheet	44 of 61

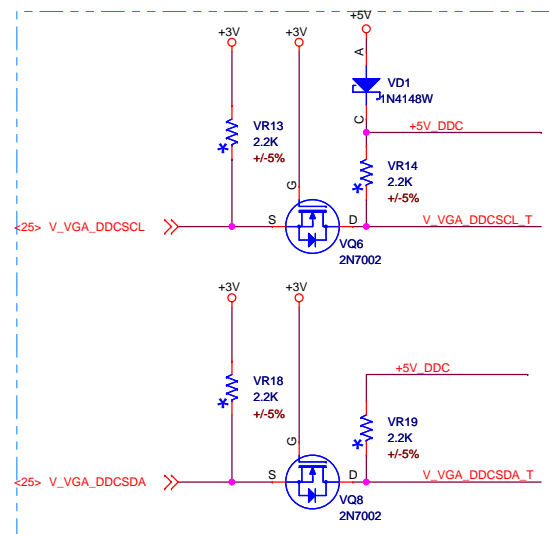


Display Port Hotplug Detect

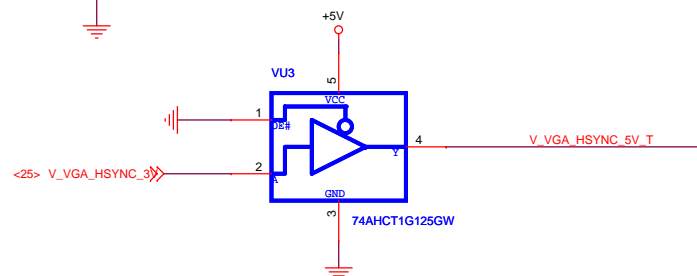
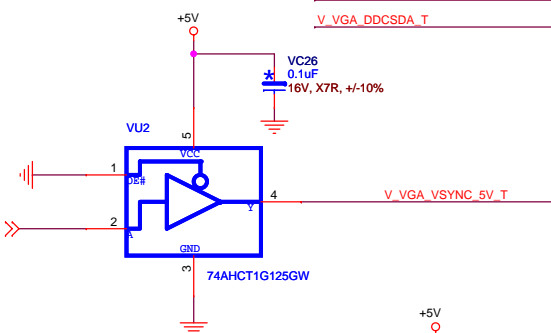
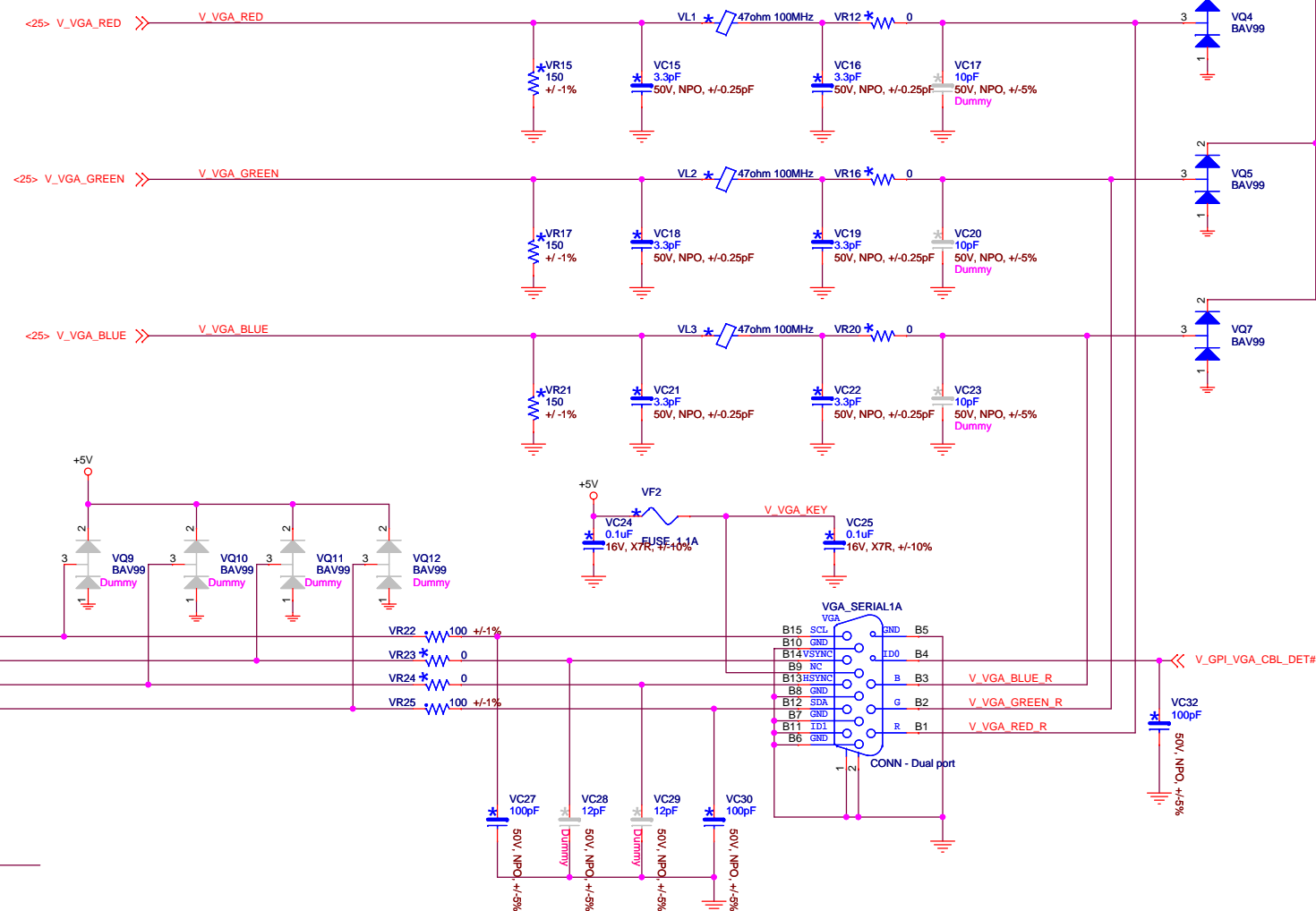


Title		DISPLAY PORT	
DWG NO	Wembley_MT		Rev A01
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VGA Connector



9/18: Modified #61



Title

VGA Connector

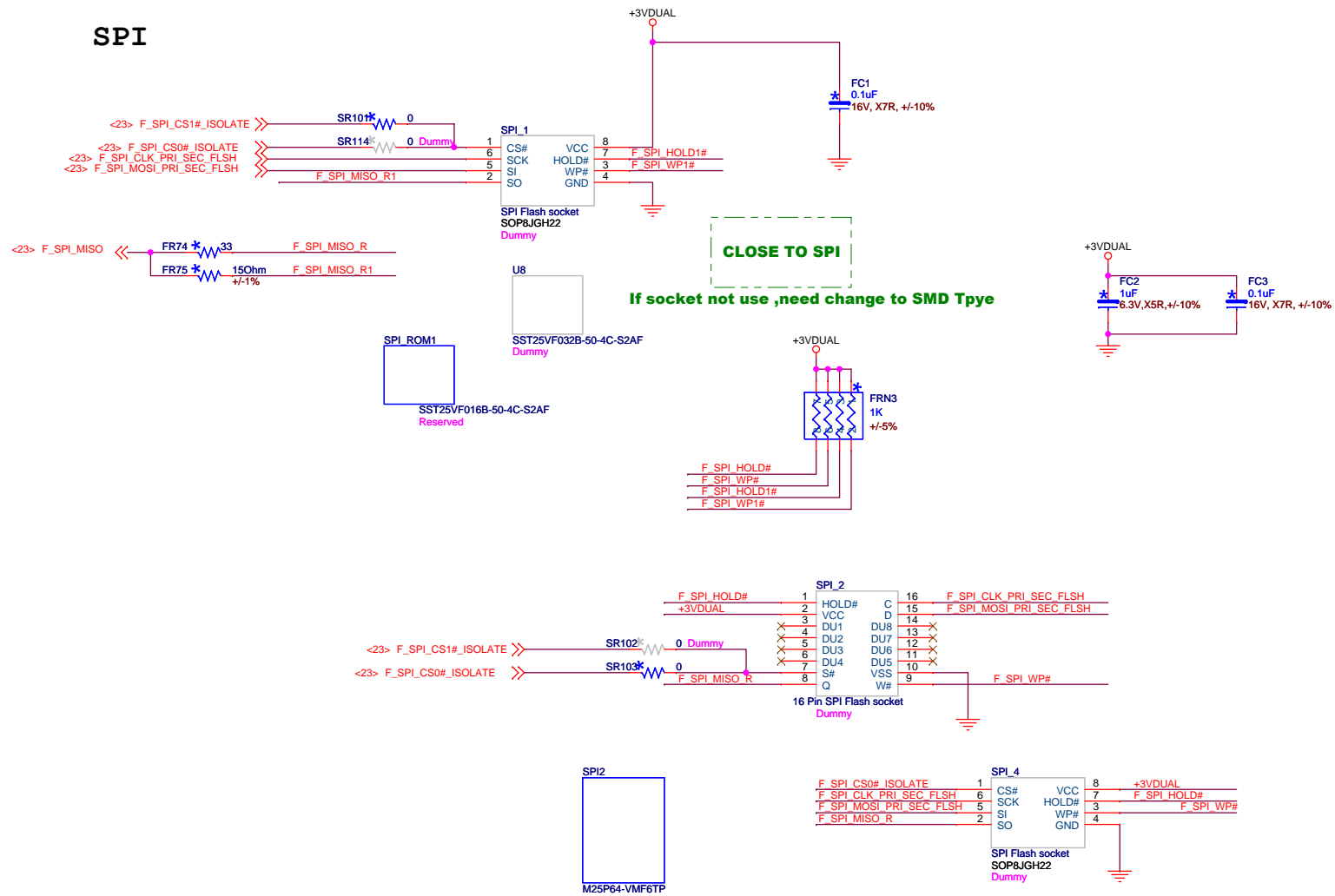
DWG NO	
--------	--

Wembley_MT

A01

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SPI

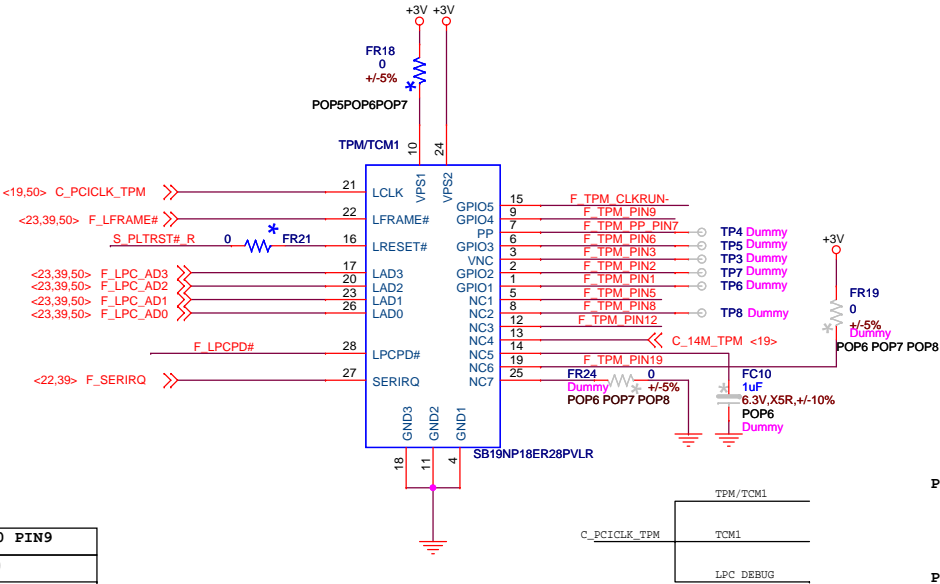
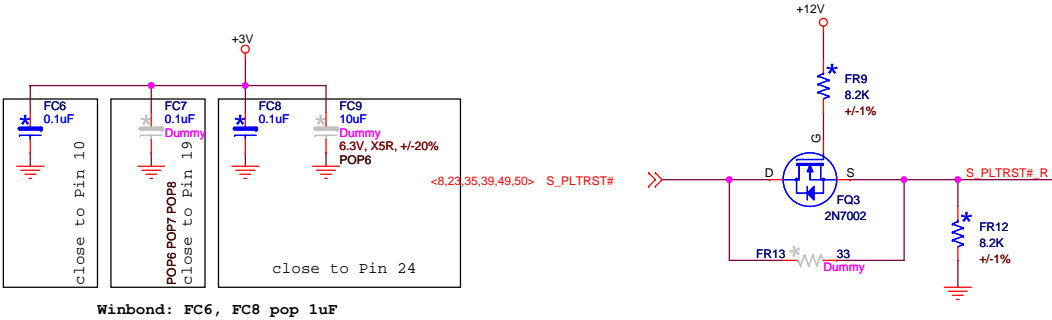


TPM, TCM

(Default) ST Micro	POP5	FR18,FR32,FR37
ZTE	POP6	FR18,FR24,FR32,FR35,FR36,FR37,FC7,FC9,FC10,FC11,FC12,FR19
Jetway	POP7	FR18,FR24,FR29,FR32,FR37,FC7,FR19
Winbond	POP8	FR24,FR26,FR27,FR37,FC7,FC15,FR19

14Mhz Clock Option Table (from CK.GEN or PCH)

(Default) ST Micro	From CK.GEN.	No Stuff CR98,CR194	From PCH	No Stuff CR198
ZTE	From CK.GEN.	No Stuff CR98,CR194	From PCH	No Stuff CR198
Jetway	From CK.GEN.	Stuff CR98,CR194	From PCH	Stuff CR198
Winbond	From CK.GEN.	No Stuff CR98,CR194	From PCH	No Stuff CR198



Base Address	BA1 PIN3	BA0 PIN9
EE/EF	0	0
7E/7F	0	1
2E/2F	1	0
4E/4F	1	1

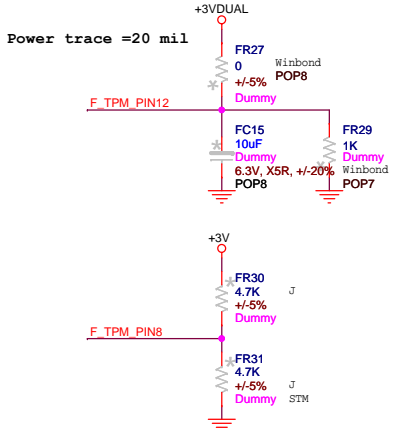
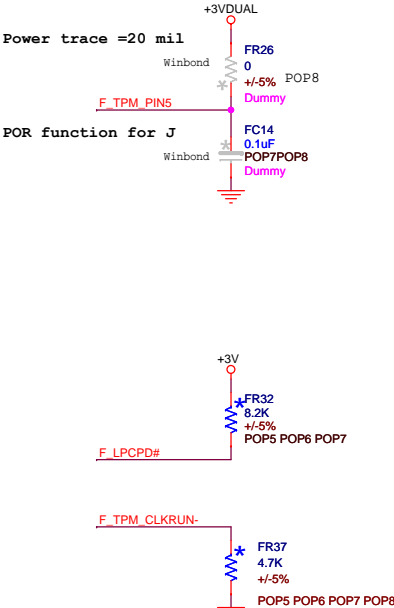
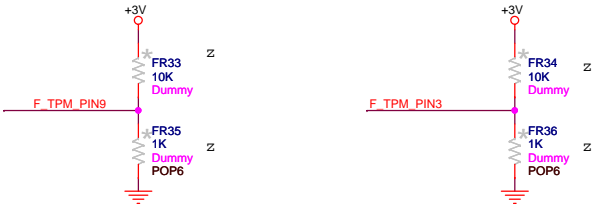
Default set EE/EF as Amy recommended, Pin 3 and Pin 9 have internal PU in Z.

STATUS	TESTEN PIN8	RUNMODES PIN9
NORMAL MODE	0	X
JTAG MODE	1	0
NORMAL MODE	1	1

J has internal PD with PIN8, internal PU with PIN9

BSEL PIN12	1(default)	0
FLASH		SRAM

J has internal PU with PIN12

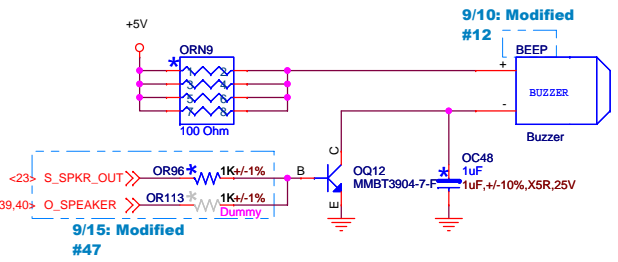


TPM & TCM

Wembley_MT

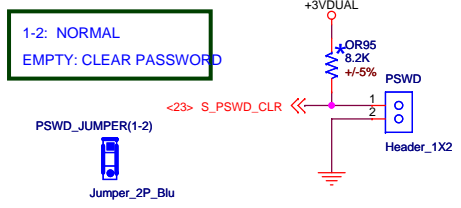
Rev A01

BEEP

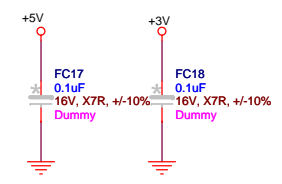
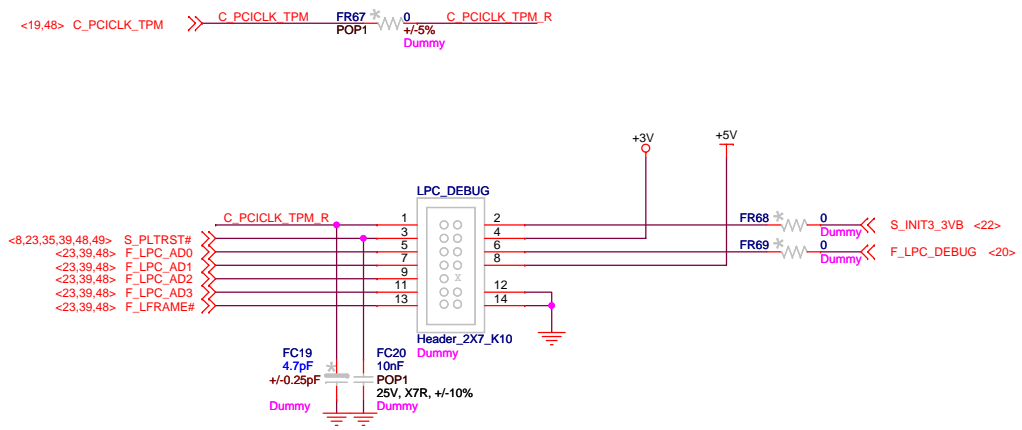


MISC Connector

Clear Password



LPC DEBUG



Title

BUZZER / CLR PSWD /LPC DEBUG

DWG NO

Wembley_MT

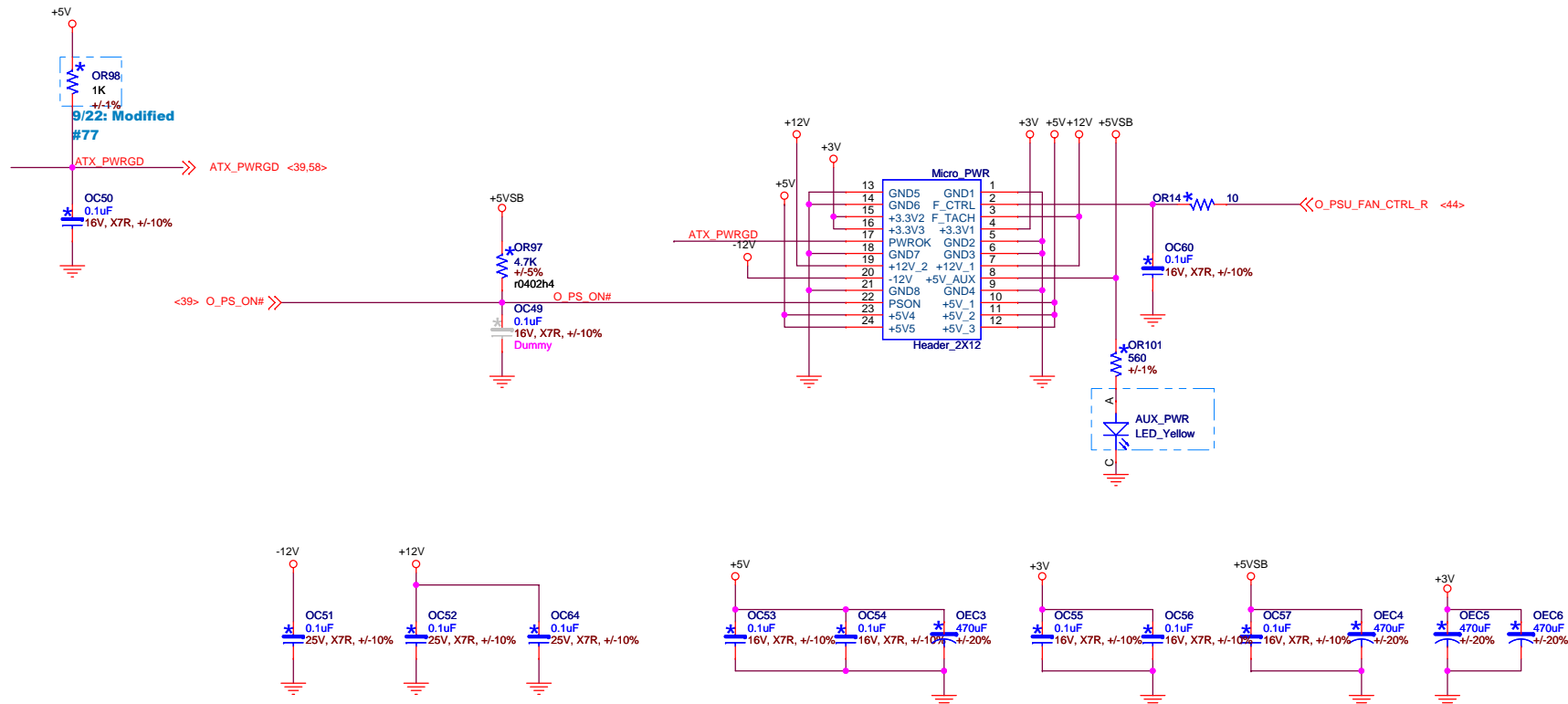
Date: Wednesday, April 14, 2010

Rev

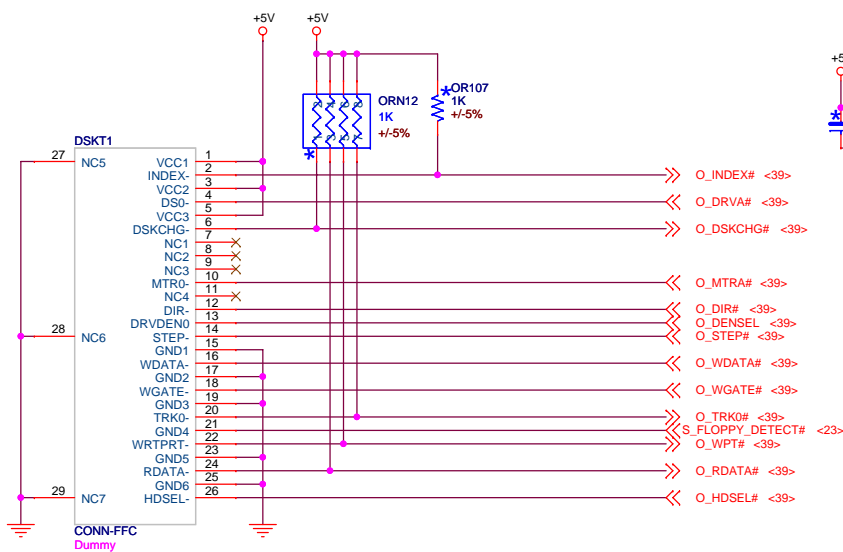
A01

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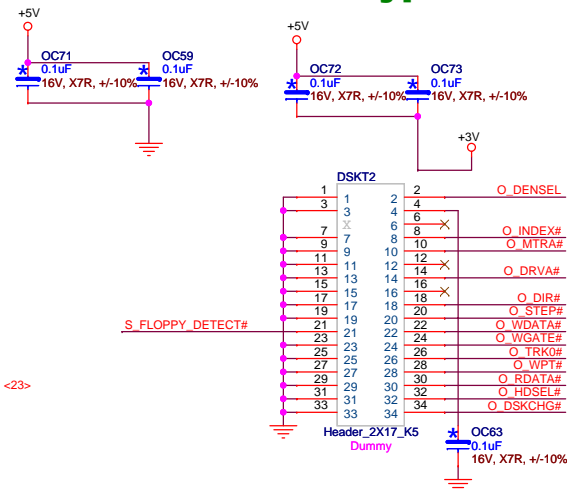
ATX POWER CONNECTOR



Slim Type @ SFF



Standard Type @ DT



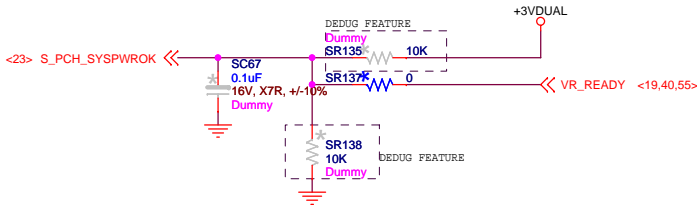
ATX POWER CONN /FDD		
DWG NO	Rev	A01
Wembley_MT		
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BACKFEED CUT

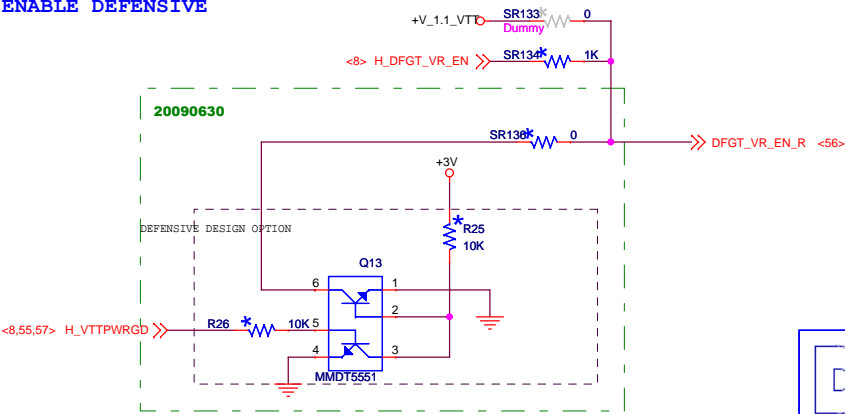
9/24: Modified #93
Remove LATCHED BACKFEED CUT Circuit

9/12: Modified #42
Remove PCIE RESET Control
Circuit

VR_READY DEFENSIVE (PCH POWEROK)



GFX VR ENABLE DEFENSIVE



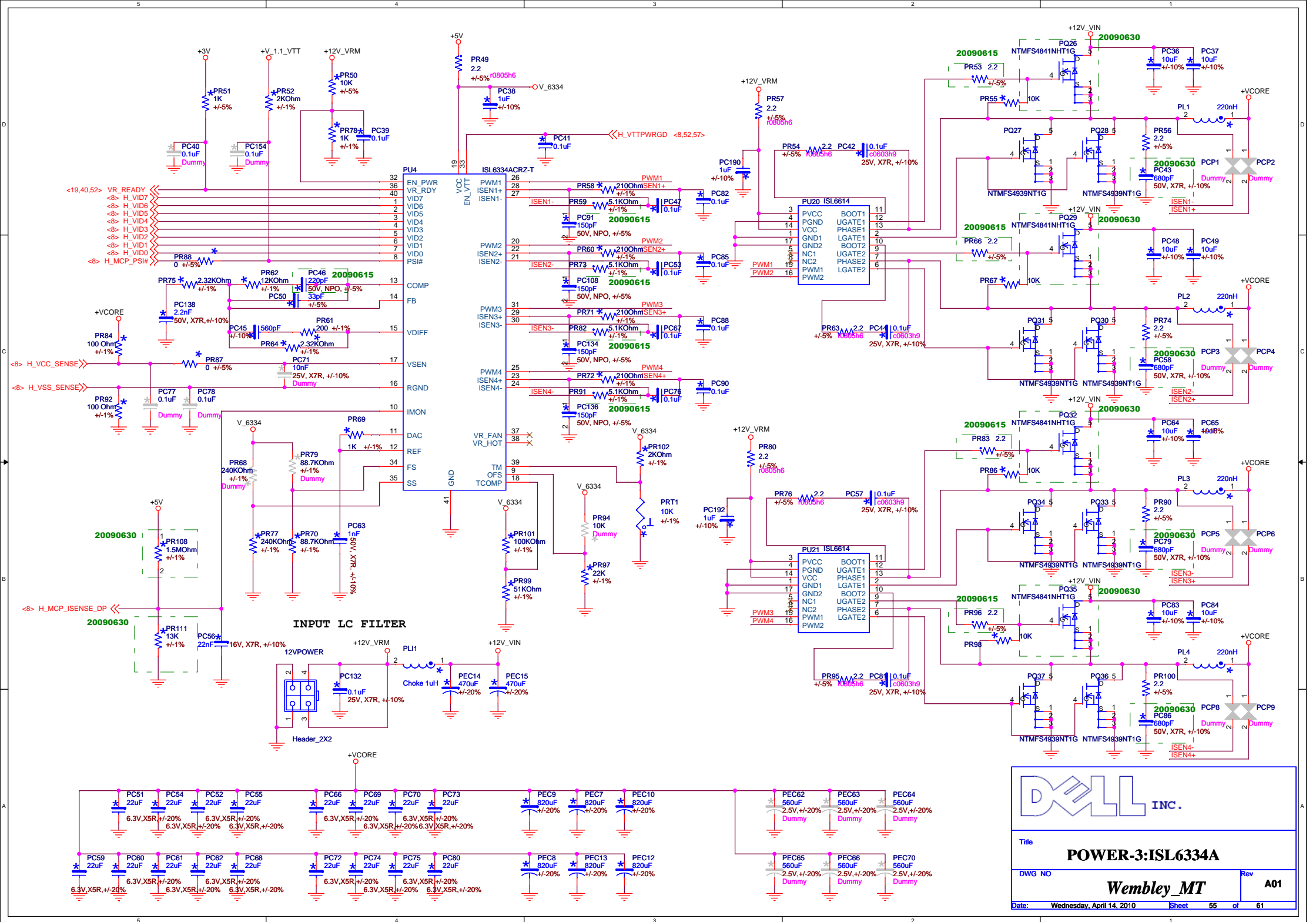
DELL INC.

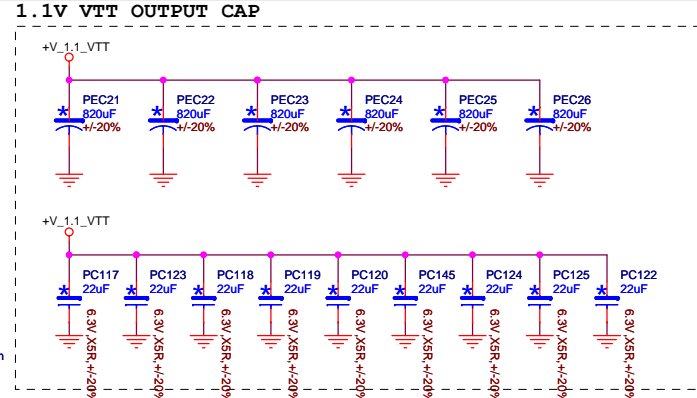
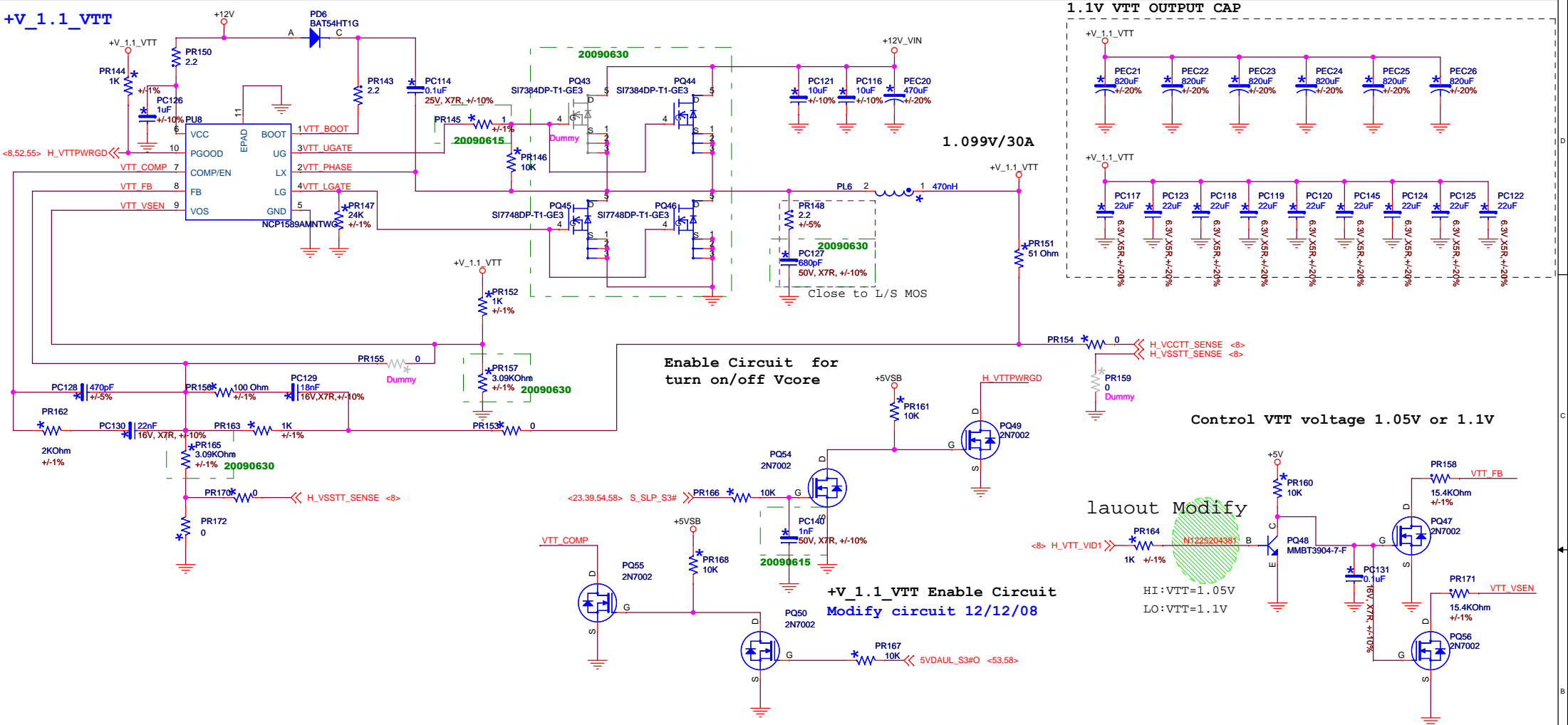
Title
POWER SEQUENCE

DWG NO
Wembley_MT

Rev
A01

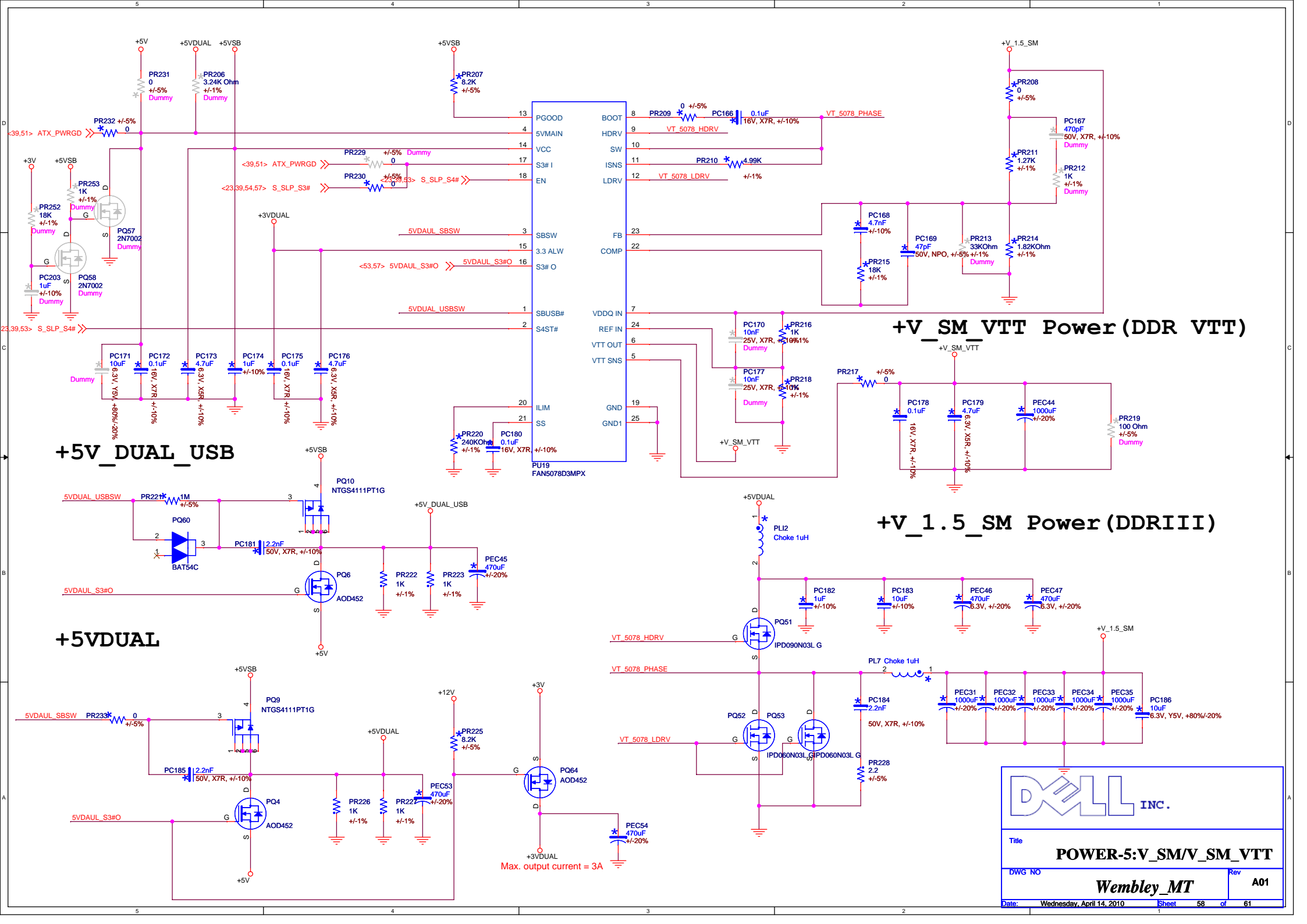
Date: Wednesday, April 14, 2010 Sheet 52 of 61





Control VTT voltage 1.05V or 1.1V

+V_1.1_VTT Enable Circuit
Modify circuit 12/12/08




+5V_DUAL_USB

+5VDUAL

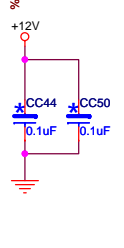
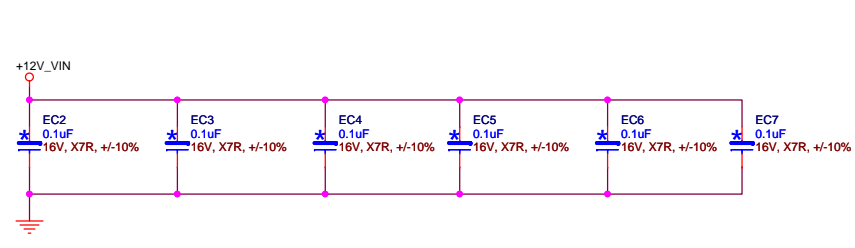
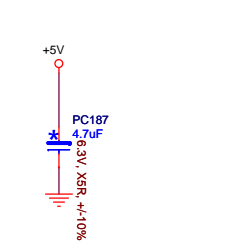
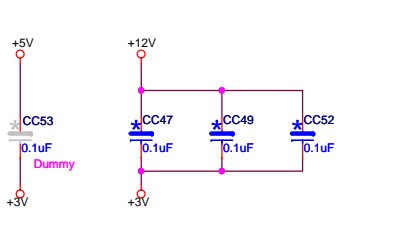
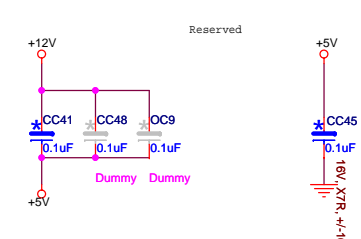
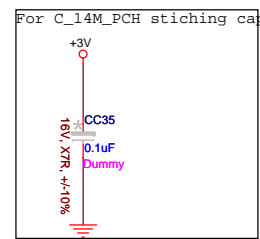
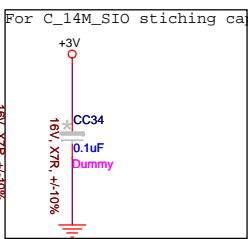
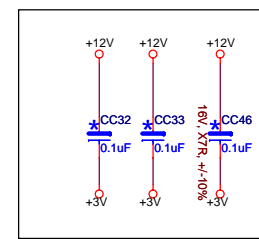
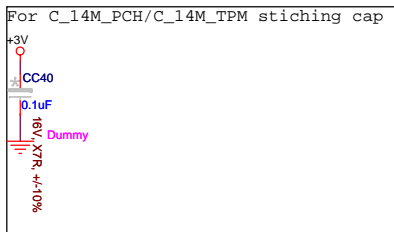
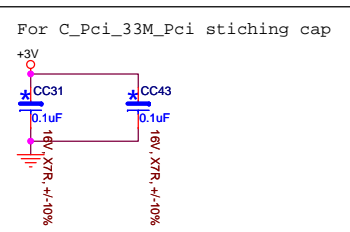
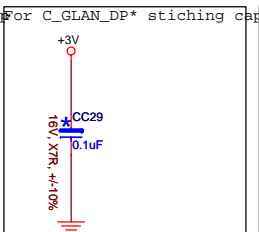
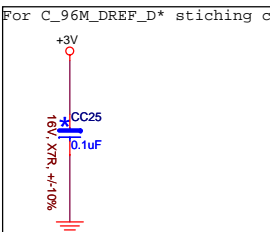
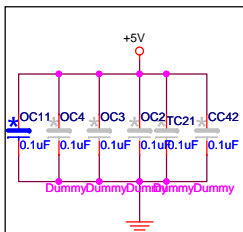
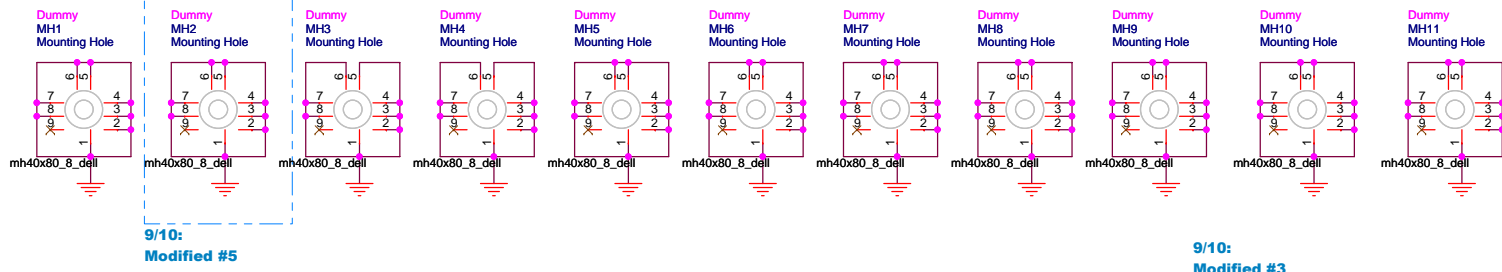
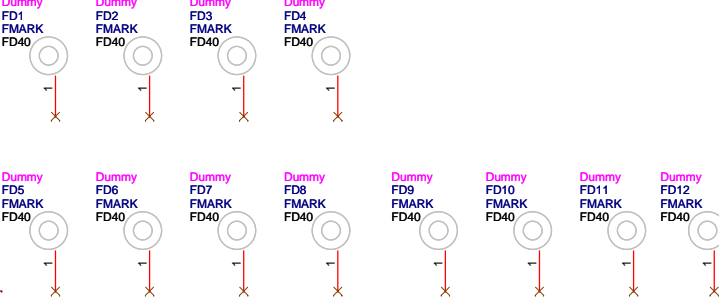
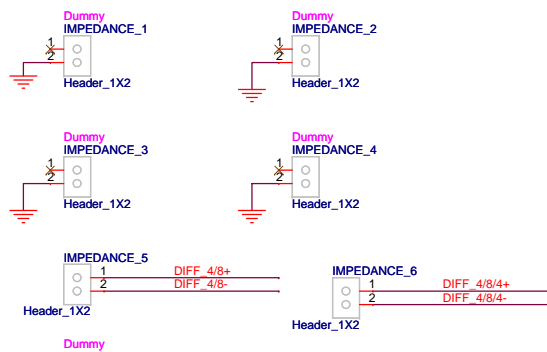
+V_SM_VTT Power (DDR VTT)

+V_1.5_SM Power (DDRIII)



INC.

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